



# Article Effective Design Methodology of CLLC Resonant Converter Based on the Minimal Area Product of High-Frequency Transformer

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**Abstract:** In DC microgrids, CLLC topology is commonly applied for battery integration. It provides galvanic separation, the ability to integrate a high-frequency transformer into the resonance circuit, and the ability to operate in a wide range of voltage. Moreover, it assures zero voltage switching conditions for all switches and zero current switching conditions for secondary side switches, which enables obtaining high efficiency. This paper presents a clear and effective approach to design a methodology for a CLLC DC/DC converter, especially a resonant tank. High-frequency transformer is fully integrated in a resonant tank. Its size is minimal and based on area product parameter  $A_p$ . An equivalent scheme for first harmonic approximation analysis is presented with inclusion of parasitic elements. Based on it, the analytical formulas are provided, which enable graphical determination of working characteristics. It was proved that the model increases the accuracy of the results. The conditions of ZVS and maximal magnetizing inductance are established, including parasitic capacitances of secondary side switches and transformer parasitic capacitances. Based on the proposed design methodology, as the proof of concept, a small-power prototype with a GaN transistor was built operating at 364 kHz. Converter losses were determined through analytical expressions and compared with the experimental and simulation results.

**Keywords:** DC/DC power conversion; bidirectional power flow; CLLC resonant converters; design methodology; GaN transistors

# 1. Introduction

The significant development of renewable energy sources (RES), electromobility, and energy storage systems (ESS) in recent years makes it necessary to look for new solutions for their safe integration into the power system. Therefore, power electronic converters become one of the most important systems that enable the modern electric power systems to operate efficiently. Every renewable energy source, microgrid, or battery system requires them to control power flow and to work properly. ESS require bidirectional converters that provide wide voltage range regulation and high efficiency. One of the most promising topologies is a CLLC resonant converter with double active bridge. The topology provides galvanic separation and enables transferring a high amount of energy in two directions while adjusting output voltage range through the transformer ratio and intrinsic voltage gain characteristic while maintaining pulse frequency modulation (PFM) control. Moreover, CLLC converters provide natural zero voltage switching (ZVS) conditions for all switches and zero current switching (ZCS) conditions for secondary side switches when the synchronous rectification and correct control algorithm is applied [1,2]. That in turn helps to minimize switching losses and EMI emissions and allows to increase switching frequency, which leads to the reduced size of magnetic and cooling elements, increasing power density at the same time.



Citation: Bartecka, M.; Kłos, M.; Paska, J. Effective Design Methodology of CLLC Resonant Converter Based on the Minimal Area Product of High-Frequency Transformer. *Energies* **2024**, *17*, 55. https://doi.org/10.3390/en17010055

Academic Editors: Antonio T. Alexandridis, Panagis N. Vovos, Konstantinos G. Georgakas and Georgios Dimitrakakis

Received: 28 November 2023 Revised: 16 December 2023 Accepted: 19 December 2023 Published: 21 December 2023



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However, the design process of CLLC resonant converters, especially dedicated to battery storage application, is still quite complicated. The difficulties, despite the typical design of power electronics converters, are mainly associated with the resonant tank and a transformer, which is a crucial part of it. CLLC topology enables to integrate leakage and magnetizing inductances of high-frequency transformer into a resonant circuit. In many studies, this feature is used to reduce the size of the magnetic elements [3-5]. Thus, the transformer parameters affect soft switching capability, gain characteristics, and finally converter efficiency. Moreover, especially for high-frequency applications, the converter design should include the influence of parasitic elements and eddy currents, wide voltage regulation capability, and possibilities of high efficiency and high power density. Numerous papers address the design methodology issue simultaneously with converter operation principle analyses [3,4,6–15]. The design process of resonant tanks usually comprises several parts: development of a mathematical model (equation formulation), selection of resonant tank parameters based on graphical operation characteristics, and, finally, resonant element fabrication (i.e., coils and/or transformer). The first stage, which usually involves the development of a mathematical model, aims to provide accurate characteristics of the device's performance. Most commonly, first harmonic approximation (FHA) is used for signal analysis [3,4,6,9,10]. The main drawback of FHA analysis, which is a decrease in accuracy for a switching frequency significantly different from the resonant frequency, is compensated for by the concise form of the mathematical equations and the simplicity of their implementation. More complex models based on time domain analysis are also being developed [8,11,12], which enable determining operation characteristics more precisely. However, the equations have a complex form and need to be formulated for each possible state of the converter [16].

Once the mathematical models are developed, the next design steps involve the selection of optimal resonant circuit elements-inductance and capacitance. The size of these components is selected on the basis of the operating characteristics of the device, which are determined graphically using developed mathematical models. The most important characteristics are voltage gain or output current as a function of switching frequency. Shapes of the characteristics vary depending on the resonant circuit parameters, such as quality factor— $Q_0$ , characteristic impedance— $Z_0$ , and ratio of resonant series inductance to parallel (magnetizing) inductance—*m*. However, performing operational characteristics in graphical form and finding the optimal solution requires first adopting the initial parameters of  $Q_0$ ,  $Z_0$ , and m. The choice of them is very wide, and recommendations for this choice are often general, complicated, or presumed. For example, in [6], symmetrical resonant circuit parameters are determined based on FHA analysis. Analytical formulas are proposed to calculate the maximum values of the quality factor, output current, and characteristic impedance, for which the gain characteristics are monotonic. Determining the maximum values of these parameters is important for the operational characteristics of the device but may lead to over-sizing the magnetic components. Moreover, the formulas are complicated and difficult to apply in practice. In [10], the design process for a symmetrical resonant circuit is also based on FHA. The maximum value of the circuit quality factor was predetermined to be 0.4. However, it should be noted that the quality factor depends on both the resonant circuit parameters, which are unknown, and load ( $Q_0 = Z_0/R_0$ ), so, for circuits with rated parameters significantly different from the proposed solution, this value does not necessarily guarantee satisfactory results. Subsequently, based on the gain characteristics, the *m* ratio and the maximum switching frequency guaranteeing the required voltage gain were selected and the remaining parameters of the resonant circuit were calculated. In [13], a design methodology for an asymmetrical resonant tank is presented based on statistical design of experiments (DoE). Firstly, analytical expressions are provided in order to guarantee desirable voltage gain and limit the maximal values of circuit quality  $Q_0$  and *m* ratio. Then, within the obtained range of  $Q_0$  and arbitrarily chosen borders of *m*, the solution is searched based on DoE. In [17], unified modeling, analysis, and design of the CLLC type are proposed. The focus is on charging and discharging parameters

relation. Once analytical expressions are based on the FHA model, gain characteristics are determined with presumed chosen quality factor  $Q_0$ . In [12], a CLLC design methodology is proposed that is based on a time domain model and parameter equivalent. Although the authors define possible operation states of the converter and provide equations to determine accurate operation characteristics, the form of them is very complex as well as the proposed process of design with their usage.

As the literature study shows, many researchers propose design methodologies of CLLC converters based on predetermined parameters of m,  $Q_0$ , and  $Z_0$ . Only in several papers is the design procedure based on very complex formulas providing precise parameter ranges. This means that the resonant tank is determined independently of the physical size of the transformer. The transformer is fabricated once the resonant tank parameters, such as  $Z_0$  and  $Q_0 m$ , are finally selected. The main difficulty in the presented approach lies in constructing components of predefined parameters, which may sometimes be unfeasible or cost a great deal of time and money. Therefore, it seems that there is still a need for a clear, effective, and practical approach to design of bidirectional CLLC converter, which reduces the pool of possible solutions and simplifies this process. The method proposed in this article is the opposite of the presented ones. First, the transformer is predesigned and fabricated and then its parameters are measured or estimated mathematically. The minimum area product  $A_{v}$  of the transformer is proposed to find the initial parameters for the high-frequency resonant tank, such as characteristic impedance  $Z_0$ , quality factor  $Q_0$ , and inductance ratio *m*. Although the area product parameter is a well-known design method for high-frequency transformer, it has never been used as a "starting point" in the design of a CLLC resonant tank. The presented approach reduces the pool of potential solutions and ensures the feasibility of the components. In addition, the paper presents a new modified FHA analysis scheme with inclusion of parasitic elements. Based on it, equations are obtained for determination of voltage gain characteristics. An improved condition for calculating maximum magnetizing inductance is also provided, with the inclusion of parasitic capacitances of transformer and switches on the secondary side.

The paper is structured as follows: Section 2 provides the research methodology, including a modified FHA model with parasitic components and equations to determine voltage gain and phase shift characteristics and power losses regarding CLLC FB converter analysis, while Section 3 presents the design methodology based on minimum area product to determine the resonant tank parameters, including parasitic components. Section 4 provides the experimental and simulation results of the developed small-power high-frequency prototype with GaN transistors and then a discussion, and Section 5 presents the conclusions.

# 2. Research Methodology

#### 2.1. FHA Model and Principles of Operation

The design methodology proposed in this paper is developed for the CLLC DAB converter. Its scheme is illustrated in Figure 1, including parasitic elements. The converter has a full bridge (FB) structure on the both sides of the high-frequency transformer. The resonant circuit is composed of primary and secondary capacitors ( $C_{rp}$ ,  $C_{rs}$ ), primary and secondary series inductances ( $L_{rp}$ ,  $L_{rs}$ ), and parallel inductance ( $L_m$ ) on the primary side. Inductances are fully integrated with high-frequency transformer, while series inductances reflect stray inductances and parallel inductance reflects magnetizing inductance. Parasitic elements are winding and core resistances and transformer capacitance and transistor on-resistances and output capacitances. It is assumed that the resonant tank is symmetrical, including transformer ratio determined as

$$\iota = N_p / N_s \tag{1}$$

where  $N_p$ —number of turns in primary winding,  $N_s$ —number of turns in secondary winding.



Figure 1. Scheme of bidirectional CLLC converter.

Thus, for the forward power flow, the equivalent resonant elements transferred for the primary side are  $L_{rp} = L'_{rs} = n^2 L_{rs}$ ,  $C_{rp} = C'_{rs} = C_{rs}/n^2$ . In the backward mode, the primary side elements are transferred to the secondary side in a similar manner. In the forward mode (FM), the primary side FB is generating high-frequency voltage, while secondary side FB is rectifying. In the backward mode (BM), the operation is opposite.

# 2.2. FHA Circuit Scheme Equivalent

First harmonic approximation (FHA) is one of the most popular methods in resonant circuit signal analysis. Since impedance of the resonant tank strongly depends on the frequency, it is assumed that the circuit responds mainly on the basic component of the input square signal, while, for other higher frequencies, it works as a filter. The theory is reliable for switching frequency close to resonant frequency. If the switching frequency is highly reduced, the secondary side resonant current becomes discontinuous and the results are not so accurate. Nevertheless, thanks to FHA, it is possible to determine the operation characteristics of the device, including voltage gain and current in function of resonant parameters and switching frequency, and formulate closed equations, which greatly simplify the design procedure, especially at the initial stage.

In Figure 2, basic FHA equivalent circuit of CLLC DAB converter is presented, where parasitic elements are omitted.



Figure 2. Basic FHA equivalent scheme of CLLC converter.

FHA equations of the basic CLLC circuit are well-known and the detailed analysis may be found, for example, in [6]. Therefore, here, only the short recall is provided. First harmonic of voltage  $v_{p1}$  obtained behind the full bridge is equal to (2) and its rms value to (3).

$$v_{p1}(t) = \frac{4V_g}{\pi}\sin(\omega_s t) = V_{p1}\sin(\omega_s t)$$
(2)

$$V_{p1_{rms}} = \frac{2\sqrt{2}V_g}{\pi} \tag{3}$$

where  $V_g$ —grid voltage,  $v_p$ —square voltage behind switching network,  $\omega_s$ —switching angular frequency,  $v_{p1}$ —first harmonic component of voltage behind the switching network.

The fundamental component of the primary resonant current can be described by Formula (4), and the average value of the input current at the midpoint of the period can be expressed by Formula (5).

$$i_{p1}(t) = I_{p1}\sin(\omega_s t - \phi_p) \tag{4}$$

$$\left(i_g(t)\right)_{T_s/2} = \frac{2}{\pi} I_{p1} \cos(\phi_p) \tag{5}$$

where  $T_s$ —switching period,  $\phi_p$ —phase shift between current and voltage at the output of primary side full bridge.

The signals at the output of resonant tank can be approximated similarly, including transformer turn ratio n. First harmonic of voltage is equal to (6) and its rms value is equal to (7). It is assumed that filtering circuit at the output of secondary FB is effective; voltage and current in DC stage ( $I_b$ ,  $V_b$ ) are constant in time. Current at the output of resonant tank is determined by (8).

$$v_{r1}(t) = nV_{r1}\sin(\omega_s t - \phi_s) = \frac{n \cdot 4V_b}{\pi}\sin(\omega_s t - \phi_s)$$
(6)

$$V_{r1_{rms}} = \frac{n \cdot 2\sqrt{2}V_b}{\pi} \tag{7}$$

where  $\phi_s$ —phase shift between current and voltage at the output of resonant tank.

$$i_{r1}(t) = I_{r1}\sin(\omega_s t - \phi_s)\frac{1}{n}$$
 (8)

Equivalent load of rectifier stage is resistor  $R'_{ac}$ , whose value is expressed by (9). Load current can be expressed by Formula (10) and equivalent resistance  $R_{ac}$  by (11), where  $R_0$  is the nominal load.

$$R'_{ac} = \frac{V_{r1}}{I_{r1}} \tag{9}$$

$$I_b = \frac{1}{n} \cdot \frac{2}{\pi} I_{r1} cos(\phi_s) \tag{10}$$

$$R_{ac} = \frac{V_{r1}}{I_{r1}} = \frac{8V_b}{\pi^2 I_b} = \frac{8}{\pi^2} n^2 R_0$$
(11)

Transfer function for circuit in Figure 2 is described as

$$H(j\omega) = \frac{Z_{pr}(j\omega)}{Z_{in}(j\omega)} \cdot \frac{R'_{ac}}{j\omega L'_{sr} + (j\omega C'_{rs})^{-1} + R'_{ac}}$$
(12)

where

$$Z_{in}(j\omega) = j\omega L_{pr} + (j\omega C_{rp})^{-1} + Z_{pr}(j\omega)$$
(13)

$$Z_{pr}(j\omega) = \frac{j\omega L_m(j\omega L'_{rs} + (j\omega C'_{rs})^{-1} + R'_{ac})}{j\omega L_m + j\omega L'_{rs} + (j\omega C'_{rs})^{-1} + R'_{ac}}$$
(14)

Voltage gain in resonant circuit is determined by the transmittance modulus  $M_v$  (15) and phase shift by its argument  $\Phi_v$  (16).

$$M_v = |H(j\omega)| \tag{15}$$

$$\Phi_v = argH(j\omega) \tag{16}$$

Phase shift  $\Phi_v$  between current and voltage observed from the terminals of the primary resonant tank is essential to determine the character of the load—capacitive or inductive, and to assess possibilities of zero voltage switching (ZVS) or zero current switching (ZCS) condition.

The scheme in Figure 2 is the most commonly used. However, it is known that the influence of parasitic components can play a significant role in operation principles of the converter [18]. In Figure 3, a new modified equivalent scheme is proposed, including parasitic elements. The expressions for the electrical signals stay the same, while the impedances of the resonant circuit are changed.



**Figure 3.** FHA equivalent scheme with parasitics of CLLC converter;  $R_p$ —equivalent resistance of all elements on primary side: windings and transistors;  $C_w$ —equivalent capacitance of transformer;  $R_{Fe}$ —resistance reflecting core losses;  $R_s$ —equivalent resistance of secondary side.

For the equivalent scheme with parasitic elements, transfer function is described by the following equation:

$$H_{par}(j\omega) = \frac{Z_{p1}(j\omega)}{Z_{in}(j\omega)} \cdot \frac{Z_{p2}(j\omega)}{j\omega L_{rp} + Z_{p2}(j\omega)} \cdot \frac{R'_{ac}}{j\omega L'_{sr} + (j\omega C'_{rs})^{-1} + R'_{s} + R'_{ac}}$$
(17)

where

$$Z_{p1}(j\omega) = \frac{j\omega L_{rp} + Z_{p2}(j\omega)}{j\omega C_w(j\omega L_{rp} + Z_{p2}(j\omega)) + 1}$$
(18)

$$Z_{p2}(j\omega) = \frac{(R_{Fe} + j\omega L_m) + (j\omega L'_{sr} \cdot (j\omega C'_{rs})^{-1} + R'_s + R'_{ac})}{(R_{Fe} + j\omega L_m)(j\omega L'_{sr} + (j\omega C'_{rs})^{-1} + R'_s + R'_{ac}) + (R_{Fe} \cdot j\omega L_m)}$$
(19)

$$Z_{in}(j\omega) = (j\omega C_{rp})^{-1} + R_p + Z_{p1}(j\omega)$$
<sup>(20)</sup>

$$M_{V_{par}} = |H_{par}(j\omega)| \tag{21}$$

$$\Phi_{v_{par}} = argH_{par}(j\omega) \tag{22}$$

Resonant circuit is characterized by additional parameters, like resonant frequency  $f_r = 1/(2\pi\sqrt{L_{rp}C_{rp}})$ , characteristic impedance  $Z_0 = \sqrt{L_{rp}/C_{rp}}$ , quality factor  $Q_0 = Z_0/R'_{ac}$ , and inductance ratio  $m = L_{rp}/L_m$ , whose significance is discussed in the following sections.

#### 2.3. Principles of Operation

CLLC converter has the natural ability to provide soft switching of the switches. If the equivalent input impedance  $Z_{in}$  is inductive, then the switches of primary side are switched on under zero voltage, which greatly eliminates switching losses. The secondary side switches are switched off under zero current if the switching frequency is lower or equal  $f_r$ . However, switching frequency lower or equal to resonant frequency is not sufficient condition to ensure ZVS. Additionally, the resonant current on primary side has to be greater than zero at the beginning of dead time to overcharge parasitic capacitances of switches and transformer. Similar analyses are completed in [10,18,19] for different resonant converters. The equivalent circuit during the period of dead time is illustrated in Figure 4. For the simplicity of the analysis, it is assumed that

- switching frequency is equal to the resonant frequency;
- magnetizing inductance is viewed as the current source;
- magnetizing current is equal to primary current and remains constant during dead time (Figure 5).



Figure 4. Equivalent scheme during dead time in forward mode (FM).

Taking into account above assumptions, operation of the equivalent circuit in Figure 4 during dead time in forward mode may be described by Formulas (23)–(25).

$$i_{L_{rs}} = i_{C_{rs}} = C_{rs} \frac{dV_{C_{rs}}}{dt} = 0$$
(23)

$$V_{L_{rs}} = L_{rs} \frac{di_{L_{rs}}}{dt} = 0 \tag{24}$$

$$0 = V_{CD} + V'_{L_{rs}} + V'_{C_{rs}} - V_{L_m} \to V_{L_m} = V_{CD}$$
<sup>(25)</sup>

where  $V'_{L_{rs}} = nV_{L_{rs}}$  and  $V'_{C_{rs}} = nV_{C_{rs}}$ .

From the principle of charge conservation in time, the following expression is formulated:

$$I_{Lm_{max}} = \frac{2V_g C_{oss_{pr}} + \Delta V_{CD} C_w + 2n V_b C_{oss_{sec}} / n^2}{t_d}$$
(26)

where  $\Delta V_{CD} = 2nV_b$ .

Magnetizing current is equal to

$$v_{Lm} = L_m \frac{di}{dt} \longrightarrow I_{Lm_{max}} = \frac{nV_b \cdot (T/2 - t_d)}{2L_m}$$
(27)

By substituting Equations (26) and (27) with the sides, and assuming a transformer ratio n, the maximum magnetizing inductance should satisfy Equation (28) in forward mode and Equation (29) in backward mode. The calculated inductances are viewed from the supply side for the given mode of operation. Correct operation of the circuit in both modes of operation will be ensured by the smaller value of the calculated magnetizing inductances converted to the same side of the transformer.

$$L_{m_{max}frd} = \frac{t_d(T/2 - t_d)}{4(C_{oss_{pr}} + C_w + C_{oss_{sec}}/n^2)}$$
(28)

$$L_{m_{max}bck} = \frac{t_d(T/2 - t_d)}{4(C_{oss_{sec}} + C_w n^2 + C_{oss_{pr}} n^2)}$$
(29)

Due to the symmetrical control of the switch pairs lying on the diagonals, the converter performance in the first half of the switching period is the same as in the second half of

the cycle for the complementary pair. The operation in both directions of power flow is symmetrical. With reference to Figure 5, the operation is as follows:

- 1. at time  $[t_0 t_1]$ , transistors A1 and D1 on the primary side and A2 and D2 on the secondary side are turned on, providing synchronous rectification. During this time, the circuit resonates at the frequency specified for the series inductance  $L_{rp}$  and the resonant capacitance  $C_{rp}$  of the primary side.
- 2. at time  $t_1$ , the secondary-side current reaches zero and switches A2 and D2 are turned off under ZCS conditions. At time  $[t_1 t_2]$ , switches A1 and D1 continue to conduct, and the resonant current is equal to the magnetization current, which increases linearly until time  $t_2$ .
- 3. at time  $t_2$ , switches A1 and D1 are turned off, and the dead time  $t_d [t_2 t_3]$  begins. The magnetizing current reaches its maximum value, increasing linearly from negative to positive peak value during  $[t_0 t_2]$  (equal to  $T/2 t_d$ ). The voltage at  $L_m$  at the moment  $t_2$  decreases from a positive to a negative value approximately equal to the input voltage modulus. The inductance  $L_m$  enters to resonance. At this time, the magnetizing current charges the output capacitances of switches A1 and D1, and the voltage across the switches increases from zero to the maximum voltage. For the complementary pair of transistors (B1 and C1), the current discharges the capacitances of the switches, and the voltage drops to zero. This makes it possible to turn on the transistors under ZVS conditions. At the same time, the parasitic capacitance of the switches are overcharged.
- 4. at time  $t_3$ , the second half period begins. The complementary pairs of switches are switched, and the resonant current changes direction.



Figure 5. Signals of CLLC converter in FM.

#### 2.4. Loss Analysis

# 2.4.1. Conduction Losses of Switches

Conduction losses result from current flow through all resistance elements. The value is proportional to square of rms current and resistance. For DAB conduction, losses in switches are the effects of on-resistance and can be calculated by

$$P_{on-t} = 2 \cdot I_{pr-rms}^2 \cdot R_{dson-pr} + 2 \cdot I_{sec-rms}^2 \cdot R_{dson-sec}$$
(30)

where

$$I_{pr-rms} = \frac{V_{p1_{rms}}}{|Z_{in}(j\omega)|} = \frac{\frac{2\sqrt{2}V_g}{\pi}}{|Z_{in}(j\omega)|}$$
(31)

$$I_{sec-rms} = n \frac{V_{p1_{rms}}}{|Z_{in}(j\omega)|} \frac{|Z_{tr}|}{|Z_{tr}| + |j\omega L'_{sr} - j\frac{1}{\omega C'_{rs}} + R'_{s} + R'_{ac}|}$$
(32)

$$Z_{tr}(j\omega)| = |\frac{R_{Fe}X_{Lm}}{R_{Fe} + X_{Lm}}|$$
(33)

where  $i_{pr}$ —rms primary side current,  $R_{dson-pr}$ —on-state resistance of primary side switches,  $i_{sec}$ —rms secondary side current (neglecting parasitic capacitance of transformer  $C_w$  due to its small value),  $R_{dson-sec}$ —on-state resistance of secondary side switches.

# 2.4.2. Driver Lossess

Lossess in driver circuits are rather low and represent a small fraction compared to total losses of the converter. In GaN transistor, driver losses are associated with recharging input charge of a gate:

$$P_g = f_{sw} Q_g V_g \tag{34}$$

where  $f_{sw}$ —switching frequency,  $Q_g$ —gate charge,  $V_g$ —gate voltage.

However, total losses in driver circuit includes also losses in integrated circuit [20]:

$$P_{dr} = V_{DDI}I_{DDI} + 2V_{DDI2}I_{DDI2} + f_{sw}Q_gV_{DD2}\frac{R_p}{R_p + R_g} + f_{sw}Q_gV_{DD2}\frac{R_n}{R_n + R_g} + 2f_{sw}C_{int}V_{DD2}^2$$
(35)

where  $V_{DDI}$ —driver input supply,  $I_{DDI}$ —input leakage current,  $V_{DDI2} = V_g$ —driver output supply,  $I_{DDI2}$ —output leakage current,  $f_{sw}$ —switching frequency,  $Q_g$ —gate charge,  $C_{int}$ —driver input parasitic capacitance,  $R_g$ —external gate resistor,  $R_p$ —driver pull-up resistor,  $R_n$ —driver pull-down resistor.

# 2.4.3. Switching Losses

Switching losses in proposed converter occur only during switching off of grid side transistors, while during switching on the ZVS conditions are held [4]:

$$P_{off} = \frac{VIt_{off}f_{sw}}{2} \tag{36}$$

where *I*—current during switching off, *t*<sub>off</sub>—switching off time, *V*—drain-source voltage.

#### 2.4.4. Transformer Losses

Transformer losses comprise core losses  $P_{Fe}$ , winding losses  $P_{Cu}$ , and additional losses  $P_{add}$ :

$$P_t = P_{Fe} + P_{Cu} + P_{add} \tag{37}$$

Winding losses are proportional to square of rms current flowing through them and effective ac resistance of particular winding. The proposed two-winding single-phase transformer can be calculated by formula:

$$P_{Cu} = i_{pr-rms}^2 R_{eff-pr} + i_{sec-rms}^2 R_{eff-sec}$$
(38)

where  $R_{eff}$ —effective resistance of winding for high-frequency current flow.

To calculate losses in Litz wires, Formula (39) may be used [21]. The calculations are reliable if skin depth is not less than diameter of a single wire in a bundle  $d_s \leq \delta$  and assuming that the field intensity increases linearly as the winding is wound and is constant across the width of the section.

$$P_{Litz} = I_{rms}^2 R_{DC} F_r \tag{39}$$

where  $F_r$  ratio of DC resistance  $R_{DC}$  rises due to eddy currents of high-frequency determined by [21]

$$F_r = 1 + \frac{(\pi \omega \mu_0 N_s n_l)^2 d_s^6 k}{768 (\rho_c b_c)^2}$$
(40)

where  $\omega$ —angular frequency of current,  $N_s$ —number of turns in a section,  $n_l$  —number of wires in a bundle,  $d_s$ —wire diameter,  $\rho_c$ —resistivity of the conductor material (copper),  $b_c$ —width of core winding window, k—factor associated with the magnetic field distribution (normally equal to 1).

Losses in a core result mainly from core magnetization (changes in a hysteresis loop) and eddy currents. Losses in a core are usually described by Steinmetz equations, whose basic version is described by the relation (41). The basic equation has limitations, such as being applicable only for sinusoidal excitation without DC offset, and does not take into account the effect of temperature changes. However, it is still readily used for basic loss estimation since the coefficients can be easily found in the manufacturer's data or determined empirically. Therefore, we decided to use basic Steinmetz formula for core loss calculations in our study.

$$P_v = k f^{\alpha} B^{\beta} \tag{41}$$

where  $P_v$ —averaged power loss per unit volume, *f*—frequency of magnetic induction changes, *B*—peak value of magnetic induction, *k*,  $\alpha$ ,  $\beta$ —material constants.

#### 3. Design Methodology

3.1. Input Data

The proposed methodology of CLLC converter design is illustrated in the graphical form in Figure 6.

The first step during CLLC converter design should be defining electrical parameters of input and output sides, including required ranges of their changes according to operation principles of batteries or power supply. The following criteria should be taken into account:

- nominal power and power range;
- input and output voltage ranges;
- nominal input and output current;
- resonance frequency.

Based on voltage ranges minimal  $M_{V_{min}}$  and maximal  $M_{V_{max}}$ , voltage gain should be calculated for both forward and backward mode:

$$M_{V_{min}-FM} = \frac{nV_{b-min}}{V_{g-max}}$$
(42)

$$M_{V_{max}-FM} = \frac{nV_{b-max}}{V_{g-min}}$$
(43)

$$M_{V_{min}-BM} = \frac{V_{g-min}}{nV_{h-max}} \tag{44}$$

$$M_{V_{max}-BM} = \frac{V_{g-max}}{nV_{b-min}} \tag{45}$$

where *n*—transformer ratio,  $V_{b-min}$ —minimal battery voltage,  $V_{g-max}$ —maximal grid voltage,  $V_{b-max}$ —maximal battery voltage,  $V_{g-min}$ —minimal grid voltage.



Figure 6. Methodology of CLLC converter design.

Further, switches of bridges in both sides should be chosen. The values of parasitic effective output capacitance  $C_{oss}$  and resistance during on-state  $R_{DS-on}$  should be reported.

# 3.2. Transformer Design

Proposed design methodology based on area product is used in this article for single phase devices; therefore, it is recommended to apply it to small-power (up to 3–4 kW) converters with transformer windings created from Litz wire.

The first step during transformer design should be the choice of core material. Further, the appropriate core shape should be selected. The criteria of maximum frequency range, core losses, maximum induction, and EMI emissions should be taken into account during the core selection.

The maximum steady-state induction flux for odd harmonics, which is contained in the transformer input signal, is expressed by the relation (46), which leads to the formula for the minimum number of primary windings (47).

$$\Phi_{max} = \frac{4V_g}{N\pi\omega} \sum_{k=1}^{\infty} \frac{1}{(2k-1)^2} = B_{max}A_c$$
(46)

$$N_p = \frac{2V_g}{\pi^2 f B_{max} A_c} \sum_{k=1}^{\infty} \frac{1}{(2k-1)^2}$$
(47)

$$n_1 = \frac{k\delta^2 b}{N_{ts}} \tag{48}$$

where k—a constant calculated according to (49),  $N_{ts}$ —the number of turns in the section, b—the width of the section from the cross-section in which one winding is in contact with the other.

$$k = \frac{\sqrt{192(F_R - 1)}}{\pi d_s^3} \tag{49}$$

where  $F_r$  is the coefficient of conductor resistance increase at high frequency, determined by the relation (40), and  $d_s$  is a single strand diameter.

The final number of strands in the bundle should be within  $\pm 25\%$  of the resulting value.

The cross-sectional area of the primary  $(A_{pwa})$  and secondary  $(A_{swa})$  windings are, respectively, defined by the formulas:

$$A_{pwa} = N_p A_{wp} \tag{50}$$

$$A_{swa} = N_s A_{ws} \tag{51}$$

where  $A_{wp}$ —cross-section of primary winding wire,  $A_{ws}$ —cross-section of secondary winding wire.

The available area of the winding window  $W_a$  is determined by the manufacturer and already takes into account the area limitation due to a bobbin. In addition, non-filling of the space due to the circular shape of conductors, insulation of conductors, insulation of winding layers, etc., must be taken into account. In summary, it is recommended to assume a window fill factor  $k_u = 0.4$ –0.6 of the available area  $W_a$ :

$$W_a k_u \ge N_p A_{pwa} + N_s A_{swa} = N_p A_{pwa} + \frac{N_p}{n} A_{swa}$$
(52)

By substituting Formula (47) for the number of turns of the primary windings and  $N_s = N_p/n$  for the number of turns of the secondary side, the relationship for the area product  $A_p$  (53) is obtained, which is by definition the product of window area and core cross-section area.  $A_p$  is usually specified in [cm<sup>4</sup>], so, when converting the cross-sectional area of the core from meters to centimeters, the numerator is multiplied by 10<sup>4</sup>, obtaining:

$$W_a A_c = A_p \ge \frac{10^4 (A_{wp} + \frac{A_{ws}}{n})}{k_u} \frac{2V_g}{\pi^2 f B_{max}} \cdot \sum_{k=1}^{\infty} \frac{1}{(2k-1)^2}$$
(53)

Thus, knowing the core material and maximum saturation induction, resonant frequency, transformer ratio, and input voltage, the minimum value of the parameter  $A_p$  can be calculated, which is generally available in manufacturers' catalogs.

After selecting the core geometry, material, and the smallest size satisfying the condition (53), the minimum number of primary side windings can be calculated according to Formula (47) taking into account the cross-section of the column of the selected core  $A_c$ . Then, the number of secondary side turns ( $N_p/n$ ) can be calculated. Obtaining an integer number for the secondary side windings may require changing the number of primary side windings. In this case, the two values must be adjusted accordingly to match the transformer's turn ratio. The ratio calculated in this way is ideal and may differ from the actual ratio. The selected core must meet the condition (52) for the modified number of turns, and, if necessary, a larger size from the series should be selected.

At this stage, the leakage inductances can be initially estimated. In many publications, the appropriate formula for the calculations is provided [23–25]. Increasing the number of winding sections reduces eddy currents associated with the proximity effect but at the same time reduces the leakage inductance. In contrast, the lack of sectioning increases the leakage inductance, which can play an important role for CLLC converters. At applications of low power, high frequencies, and low voltages, leakage inductance will be low, so sectioning may not be advisable. In contrast, at high power, low frequencies, and high voltages, the leakage inductance without sectioning of the winding may be too high. Thus, depending on the power range, resonant frequency, and voltage, a final decision has to be made on the winding arrangement. The most reliable values of transformer leakage inductance for further simulations and experiments can be obtained by measuring a preliminary constructed transformer. Also, measuring parasitic capacitance of a preliminary fabricated transformer is the best way to obtain an accurate model.

As already mentioned, in CLLC converters, the magnetizing inductance plays a significant role in determining voltage gain characteristics and affects the system efficiency. So, firstly, it should be limited to provide ZVS conditions for the switches according to (28). Then, the magnetizing inductance, with respect to the leakage inductance, should be chosen to provide required voltage gain.

#### 3.3. Resonant Capacitance

The resonance capacitors of the primary and secondary sides are calculated from the series resonance relationship for the estimated leakage inductances of the primary and secondary sides, respectively:

$$C_{rp} = \frac{1}{(2\pi f_r)^2 L_{rp}}$$
(54)

$$C_{rs} = \frac{1}{(2\pi f_r)^2 L_{rs}}$$
(55)

# 3.4. Transfer Function

Based on the FHA equivalent scheme in Figure 3 and Equations (21) and (22), the voltage gain characteristics and impedance character may be determined. The most reliable characteristics will be obtained for already-built and measured transformer. In Figures 7 and 8, voltage gain characteristics for ideal circuit without parasitic elements and circuit with parasitic elements are compared for forward and backward mode, respectively. Solid lines indicate the results for the FHA equivalent model, while the marks indicate the results of the simulations, where all parasitic elements were omitted or included. From the figures, it can be seen that, although FHA analysis in some cases does not provide accurate results, the inclusion of parasitics in simulation models and in equivalent schemes can improve the accuracy, especially in the part of frequencies significantly different than resonant. Due to the unlinear behavior of transformer voltage ratio under different load, the characteristics of FM and BM are not purely symmetrical.

In Figure 9, voltage gain characteristics in the function of the normalized frequency  $(f_s/f_r)$  and dependent on *m* ratio are presented for both backward and forward mode. Higher magnetizing inductance (lower *m*) results in more flat curve and may lead to voltage gain lower than unity in wide frequency range. However, it also increases system efficiency and reduces conduction losses.

In Figure 10, voltage gain characteristics in the function of the normalized frequency  $(f_s/f_r)$  and dependent on characteristic impedance  $Z_0$  are presented for both backward and forward mode. Higher  $Z_0$ , which defines leakage inductance higher than resonant capacitors, causes more flat gain as well and may lead to voltage gain lower than unity. Thus, increasing  $Z_0$  requires higher magnetizing inductance to provide sufficient voltage gain.



**Figure 7.** Voltage gain characteristic comparison for analytical solution (FM Id, FM Par) and simulation results (FM Id sym, FM Par sym) with and without parasitic elements in forward mode.







Figure 9. Voltage gain characteristics dependent on different *m* values.



Figure 10. Voltage gain characteristics dependent on different Z<sub>0</sub> values.

In Figure 11, voltage gain characteristics dependent on quality factor  $Q_0$  are illustrated for both backward and forward mode. Higher  $Q_0$  causes less step gain characteristics, especially in the region of lower switching frequency close to freewheeling frequency. Lower  $Q_0$  for the same resonant circuit parameters indicates lower load.



Figure 11. Voltage gain characteristics dependent on different Q<sub>0</sub> values.

# 4. Results and Discussion

In order to validate the proposed design methodology, a small-power prototype was built. The converter operates under resonant frequency equal to 364 kHz, its power is 500 W, microgrid voltage is equal to 120 V  $\pm$  5 V, while the nominal battery voltage is 48 V and its range is from 43.2 V to 54.4 V. The turn ratio of the transformer is equal to 2.5 for nominal voltage values. The converter is controlled with pulse frequency modulation (PFM) and synchronous rectification of the secondary side switches.

Switches GS66508T made of GaN were chosen for the prototype for both active bridges. This fact was due to the difficulties in obtaining GaN transistors dedicated to low voltage in the market during the COVID-19 pandemic. The  $R_{DSon}$  is equal to 65 m $\Omega$ , including temperature rise, and  $C_{oss}$  is assumed to be 500 pF for 48 V  $V_{DS}$  and 300 pF for 120 V  $V_{DS}$  [26]. For primary winding (microgrid side), Litz wire 180 × 0.1 was chosen, while, for secondary side (battery side), Litz wire 400 × 0.1 was chosen. For resonance frequency 364 kHz, the skin depth is equal 0.12 mm. Thus, the diameter of the single wire in a strand is lower than the calculated skin depth.

#### Core Choice Discussion

Following the proposed algorithm of the resonant tank design (Figure 6), after defining parameters and requirements for a converter and choosing switches, the next step is transformer design. Based on the material properties, ferrite N97 is suggested as it is a good compromise regarding price and quality for predicted frequency. However, other materials may be chosen as well. For the particular example, RM geometry is chosen as the shape provides quite good power quality with sufficient winding area. Alternatively, other core shapes, like ETD or PQ, may be selected dependent on the requirements and applications.

According to Equation (53), for the selected core material, conductor cross-sections, assumed turn ratio, resonant frequency, and corresponding saturation flux density  $B_{max}$  for the selected frequency and window fill factor equat to  $k_u = 0.4$ , the minimum core area product  $A_p$  is 1.61 cm<sup>4</sup>. The core cross-section of the selected model should be above or equal to the calculated value. The first size of RM core satisfying this condition is RM14, whose parameters are shown in Table 1.  $A_p$  of smaller core size RM12 is 1.095 cm<sup>4</sup> [27] and is not sufficient.

Parameter	Symbol	Value
Initial magnetic permeability (at 25 °C)	$\mu_i$	$2300\pm25\%$
Volume loss density in the core (at 500 kHz, 50 mT, 100 °C)	$P_{cv}  [\mathrm{kW}/\mathrm{m}^3]$	200
Saturation flux density (at 1200 A/m, 10 kHz, 100 $^{\circ}$ C)	$B_s$ [mT]	410
Curie temperature (min.)	$T_c [°C]$	>230
Core cross-section area	$A_c  [\mathrm{cm}^2]$	1.78
Core volume	$V_e$ [cm <sup>3</sup> ]	12.5
Area product	$A_p  [\mathrm{cm}^4]$	2.03
Magnetic path length	$l_c$ [cm]	0.07

Table 1. Parameters of selected core [28].

The parameters of the prototype are gathered in Table 2. The view is presented in Figure 12. The prototype is built from two identical PCBs. Driver circuits are controlled by DSP board TMS20F28335. PCBs include driving circuits, measurement circuits, and power loop. Transistors are placed on the bottom side of the boards. The gates of the transistors are driven with +6/-2 V from SI8271 drivers to ensure more robust switching conditions.

Figures 13–20 present the oscillograms of the fabricated converter. In all of them,  $V_{DS}$  and  $V_{GS}$  are the drain source voltage and gate-source voltage of the indicated transistor, respectively,  $I_{pr-rez}$ —resonant current on the grid side of the converter,  $I_{sec-rez}$ —resonant current on the battery side of the converter. Figure 13 shows steady-state signals from the prototype during forward mode under nominal load for primary side (grid side) and Figure 14 illustrates the corresponding signals on the secondary side. Figure 15 presents steady-state signals during forward mode under 10% of nominal load for the primary side (grid side) and Figure 16 illustrates the corresponding signals on the secondary side. In all the figures, the switching frequency is equal to the resonant frequency. The dead time for the primary side switches is set to 60 ns, which is sufficient time to achieve switch-on of the switches at zero voltage. On the primary side, switches are turned on under ZVS, while on the secondary

side switches are turned on and turned off under ZVS conditions. For both load levels, the switches of the secondary side are controlled as synchronous rectifiers to achieve ZCS.

Element	Value	Remarks
$C_{rp}$ [nF]	120	WIMA FKP1; No data about $R_{ESR_{eq}}$
$C_{rs}$ [nF]	622	WIMA FKP1; No data about $R_{ESR_{eq}}$
$L_m$ [ $\mu$ H]	15.2	
$L_{rp}$ [ $\mu$ H]	1.60	Core RM14, material N97
$L_{rs}$ [µH]	0.303	
$R_{eff-pr}$ [m $\Omega$ ]	48.5	multiplied by $F_{r-pr}$
$R_{eff-sec}$ [m $\Omega$ ]	41	multiplied by $F_{r-sec}$
resonant frequency [kHz]	364	switching range: 180 kHz–520 kHz
$Z_0[\Omega]$	3.65	$\sqrt{L_{rp}/C_{rp}}$
т	0.11	$L_{rp}/L_m$
$Q_0$	0.15	$Z_0/R_{ac}$
Turns ratio $N_p:N_s$	10:4	
Transistors	GS66508T	8

Table 2. Design parameters of proposed converter.



Figure 12. View of a prototype with DSP board.



**Figure 13.** Forward mode under nominal load and  $f_{sw} = f_r$  at grid side; CH1— $V_{GS}$  (10 V/div) A1, CH4— $V_{DS}$  A1 (50 V/div), CH3— $I_{pr-res}$  (10 A/div).



**Figure 14.** Forward mode under nominal load and  $f_{sw} = f_r$  at battery side; CH1— $V_{GS}$  A2 (10 V/div), CH4— $V_{DS}$  A2 (50 V/div), CH3— $I_{sec-res}$  (25 A/div).

Figures 17–20 show the main signals from the prototype operating in the steady-state backward mode at switching frequency equal to resonant frequency for the battery side and grid side. Figures 17 and 18 show the signals at nominal load, while Figures 19 and 20 illustrate signal for 30% of nominal load on both sides of the transformer. The operation of the converter is similar to the operation in forward mode. Grid side switches are now controlled as synchronous rectifier and turned off under ZCS. On both sides, switches are turned on under ZVS, and additionally on the grid side (secondary side in BM) switches are turned off under ZVS. The oscillations visible on the grid side indicate the influence of parasitic capacitance.



**Figure 15.** Forward mode under 10% of nominal load and  $f_{sw} = f_r$  at grid side; CH1— $V_{GS}$  A1 (10 V/div), CH4— $V_{DS}$  A1 (50 V/div), CH3— $I_{pr-rez}$  (10 A/div).

For the developed prototype, loss calculations were conducted based on Section 2.4. For forward mode and according to the numerical solution of Equations (31) and (32), the current values for nominal load and resonant frequency are equal to 5.4 A and 11.06 A, respectively. Conduction losses of the switches are calculated based on Formula (30) with  $R_{DSon} = 65 \text{ m } \Omega$ .

Winding losses of transformer are calculated according to Equation (38) based on the same current values as above and effective winding resistances consistent with the values in Table 2. Core losses are determined based on Formula (41) taking into account material constants ( $\alpha = 1.1145$ ,  $\beta = 2.116$ , k = 0.05), resonant frequency, and saturation flux density 50 mT.



**Figure 16.** Forward mode under 10% of nominal load and  $f_{sw} = f_r$  at battery side; CH1— $V_{GS}$  A2 (10 V/div), CH4— $V_{DS}$  A2 (50 V/div), CH3— $I_{pr-res}$  (10 A/div).



**Figure 17.** Backward mode under nominal load and  $f_{sw} = f_r$  at battery side; CH1— $V_{GS}$  A2 (10 V/div), CH4— $V_{DS}$  A2 (20 V/div), CH3— $I_{sec-res}$  (25 A/div).



**Figure 18.** Backward mode under nominal load and  $f_{sw} = f_r$  at grid side; CH1— $V_{GS}$  A1 (10 V/div), CH4— $V_{DS}$  A1 (50 V/div), CH3— $I_{pr-res}$  (5 A/div).



**Figure 19.** Backward mode under 30% of nominal load and  $f_{sw} = f_r$  at battery side; CH1— $V_{GS}$  A2 (10 V/div), CH4— $V_{DS}$  A2 (20 V/div), CH3— $I_{sec-rez}$  (25 A/div).



**Figure 20.** Backward mode under 30% of nominal load and  $f_{sw} = f_r$  at grid side; CH1— $V_{GS}$  A1 (10 V/div), CH4— $V_{DS}$  A1 (50 V/div), CH3— $I_{rez}$  (5 A/div).

Turn-off losses of grid side switches were calculated based on Formula (36). The turnoff time was assumed to be 16 ns. Since the resonant current on the primary side is equal to the magnetizing current (27) when the switches are turned off, the relation for the turn-off losses for the primary side switches is as follows:

$$P_{sw_{off}} = \frac{V_g \frac{nV_0 \cdot (T/2 - t_d)}{2L_m} t_{off} f_{sw}}{2} \cdot 4$$
(56)

Gate driver losses were determined based on the Formula (35). Data were taken according to the driver manufacturer's data sheet ( $R_p = 2.7 \text{ m}\Omega$ ,  $R_n = 1 \text{ m}\Omega$ ,  $C_{int} = 370 \text{ pF}$ ,  $I_{DDI} = 10 \text{ mA}$ ,  $I_{DDI2} = 4 \text{ mA}$ ) and transistor ( $Q_g = 6 \text{ nC}$ ) and the voltages and resistors used in the prototype ( $V_{DDI} = 5 \text{ V}$ ,  $V_{DDI2} = 8 \text{ V}$ ,  $R_g = 15 \text{ m}\Omega$ ,  $f_{sw} = 360 \text{ kHz}$ ) [20]. For eight-gate driver circuits, the total losses are equal:

$$P_{dr_{tot}} = 8P_{dr} \tag{57}$$

Losses in backward mode may be determined in a similar way, after transforming the FHA circuit on the secondary side. In backward mode, according to the commercial solution of transformed Equations (31) and (32), the current values for nominal load and resonant frequency are equal to 4.4 A on the grid side and 12.7 A on battery side. The losses determined by the analytical method are gathered in Table 3. A comparison of the device efficiencies collected through calculations, simulation results, and experiments is summarized in Table 4, where efficiency is defined as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_b I_b}{V_g I_g} \tag{58}$$

Table 3. Converter losses.

Losses	FM		1	BM	
	[W]	[%]	[W]	[%]	
Switch conduction losses (Grid)	3.8	0.76	2.52	0.5	
Switch conduction losses (Battery)	15.9	3.18	21.1	4.22	
Transformer losses	7.93	1.59	9.09	1.82	
(winding and core)					
Turn-off losses	7.26	1.45	6.72	1.34	
Driver losses	1.71	0.34	1.71	0.34	

Table 4. Comparison of converter efficiency determined in different ways under nominal load.

Efficiency	Analytical	Simulations	Experiments
FM [%]	92.68	93.5	92.54
BM [%]	91.9	92.6	91

In Figure 21, the efficiency curve for the developed prototype is presented and compared with the simulation results. The highest efficiency was gained under 45% of the nominal load, reaching 95.7% in forward mode and 91.7% in backward mode. The efficiency difference between these two modes comes from the slightly higher current in backward mode. As shown in the figure, the efficiency is not very high; however, by comparing the results with Table 3, important conclusions can be drawn. Firstly, the highest share in overall losses comes from conduction losses of the battery side switches. This is caused by the quite high switch on-resistance and high current flowing through it. The second position includes transformer losses, which can be reduced by applying different Litz wires, characterized by smaller wire size in a strand that will help to minimize eddy currents. The last position includes switching losses, which increase with increasing frequency.



Figure 21. Power converter efficiency.

In order to verify the possibility of improving efficiency, additional simulations have been completed. Switches for battery side FB were replaced by switches GS61008T based on GaN and dedicated to lower voltage (up to 100 V). *R*<sub>DSon</sub> of replaced switches is equal to

 $9 \text{ m}\Omega$ , including temperature rise. Based on analytical analysis, the change allows to reduce battery side FB conduction losses from almost 16 W to 2.22 W. The resulting efficiency curve is presented in Figure 22. The highest efficiency was 96.7% in forward mode and 96.4% in backward mode.



Figure 22. Improved power converter efficiency.

Then, in order to compare the performance of the manufactured prototype with other works, additional analysis of the state of art was carried out considering solutions with similar parameters. The results are summarized in Table 5. As Table 5 shows, the efficiency of the fabricated converter does not differ significantly from other studies. Moreover, considering Figure 22, the efficiency can be even more competitive when other switches are applied. This proves that the proposed methodology makes it possible to achieve the goal of creating a high-efficiency converter that meets the input requirements.

Topology	Power P [W]	f <sub>rez</sub> [kHz]	V <sub>in</sub> [V]	V <sub>out</sub> [V]	η [%]	Reference
CLLC	3300	130	380-400	270-430	96.5	[3]
DAB						[•]
CLLC	1000	100	90_110	100	97	[29]
DAB	1000	100	<i>y</i> 0 110	100		[27]
CLLC	1000	280 540	250 220	200	05.6	[20]
DAHB	1000	360-340	250-520	390	95.0	[30]
CLLC	500	363 kHz	120	48	95.7	this paper

 Table 5. Comparison of CLLC converters presented in the literature.

Considering the design methodology described in the literature, a few observations can be made. In [30], the preliminary selected values of the inductance coefficient and quality factor were determined. Then, on their basis, the graphical characteristics of the voltage gain were determined, on which the final selection was based. In [29], the authors choose minimal circulating current criterion to determine impedance value and inductance ratio. However, the final choice is also based on a preliminary set of values and a subjective compromise between them. In contrast, the methodology proposed in our article allows to select resonant circuit parameters based on input data and minimal area product of transformer and guarantees the feasibility of the simulated solution. Moreover, it provides the mathematical formulas to determine gain characteristics, including parasitic elements.

# 5. Conclusions

Power electronic converters play a significant role in electric power system transformation. Almost every renewable energy source, battery energy system, or microgrid requires them to operate efficiently and correctly. Therefore, the issue of designing high-efficiency power electronic converters is still topical. The article fits into this theme and presents a solution dedicated to the integration of battery energy storage systems with a DC microgrid. The article provides guidelines for designing a power electronic converter that will meet input requirements and operate with high efficiency.

In this paper, a clear, practical, and effective approach to CLLC converter design based on minimum area product is proposed. The suggested methodology enables to fully integrate resonant inductances in transformer with simultaneous minimizing magnetizing component size and increase in power density. Firstly, the equivalent model for FHA analyses with parasitic components is presented and equations to determine voltage gain and phase shift are present. The simulation results show that inclusion of parasitic elements improves the accuracy of the results, making them more reliable. Further, the power losses of the converter are analyzed and analytical formulas to determine them are provided.

The validation of the proposed methodology was assessed based on the developed prototype with a GaN transistor, operating at 364 kHz with synchronous rectification and PFM control. The power losses are calculated, and converter efficiency outcomes based on analytical calculation, simulation results, and measurements are compared.

The proposed methodology is general and may be applied for designing one-phase devices with transformer winding made from Litz wires. Hence, electrical parameters of any converter, such as voltage, frequency, and power, are taken into account for calculating the area product  $A_p$  of a designed transformer; the element is capable of transferring adequate power while minimizing the resonant circuit elements. Furthermore, the proposed methodology eliminates the problem of the technical infeasibility of a transformer with arbitrarily specified parameters for the leakage inductance and allows to significantly limit the  $Z_0$  parameter.

**Author Contributions:** Conceptualization, M.B., J.P. and M.K.; methodology, M.B.; software, M.B.; validation, J.P. and M.K.; formal analysis, J.P.; investigation, M.B.; resources, M.B.; data curation, M.B.; writing—original draft preparation, M.B.; writing—review and editing, M.K. and J.P.; visualization, M.B.; supervision, M.K. and J.P.; project administration, M.B., M.K. and J.P.; funding acquisition, M.K. All authors have read and agreed to the published version of the manuscript.

**Funding:** POWERSKIN+ Highlyadvanced modular integration of insulation, energizing and storage systems for non-residential buildings. This paper was funded by the European Union's Horizon 2020 research and innovation program under grant agreement No. 869898.

Data Availability Statement: Data are contained within the article.

Conflicts of Interest: The authors declare no conflicts of interest.

#### References

- Zou, S.; Lu, J.; Mallik, A.; Khaligh, A. Bi-Directional CLLC Converter With Synchronous Rectification for Plug-In Electric Vehicles. IEEE Trans. Ind. Appl. 2018, 54, 998–1005. [CrossRef]
- Li, B.; Chen, M.; Wang, X.; Chen, N.; Sun, X.; Zhang, D. An Optimized Digital Synchronous Rectification Scheme Based on Time-Domain Model of Resonant CLLC Circuit. *IEEE Trans. Power Electron.* 2021, 36, 10933–10948. [CrossRef]
- Liu, G.; Li, D.; Zhang, J.Q.; Hu, B.; Jia, M.L. Bidirectional CLLC resonant DC-DC converter with integrated magnetic for OBCM application. In Proceedings of the 2015 IEEE International Conference on Industrial Technology (ICIT), Seville, Spain, 17–19 March 2015; pp. 946–951. [CrossRef]
- 4. He, P.; Mallik, A.; Sankar, A.; Khaligh, A. Design of a 1-MHz High-Efficiency High-Power-Density Bidirectional GaN-Based CLLC Converter for Electric Vehicles. *IEEE Trans. Veh. Technol.* **2019**, *68*, 213–223. [CrossRef]
- Siebke, K.; Schobre, T.; Mallwitz, R. Comparison of GaN based CLLC converters for EV chargers operating at different switching frequency ranges. In Proceedings of the 2019 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe), Genova, Italy, 3–5 September 2019; pp. 1–9. [CrossRef]
- Jung, J.; Kim, H.; Ryu, M.; Baek, J. Design Methodology of Bidirectional CLLC Resonant Converter for High-Frequency Isolation of DC Distribution Systems. *IEEE Trans. Power Electron.* 2013, 28, 1741–1755. [CrossRef]
- Lv, Z.; Yan, X.; Fang, Y.; Sun, L. Mode analysis and optimum design of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems. In Proceedings of the 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, Canada, 20–24 September 2015; pp. 1513–1520.

- Wang, L.; Luo, Q.; Luo, T. A Time-Domain Optimization Design Methodology for CLLC Resonant Converter. In Proceedings of the 2021 IEEE 1st International Power Electronics and Application Symposium (PEAS), Shanghai, China , 13–15 November 2021; pp. 1–5. [CrossRef]
- Liu, M.; Wang, X.; Xu, J. Design Methodology of SiC MOSFET Based Bidirectional CLLC Resonant Converter for Wide Battery Voltage Range. In Proceedings of the 2021 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Wuhan, China, 25–27 August 2021; pp. 423–427. [CrossRef]
- 10. Liu, Y.; Du, G.; Wang, X.; Lei, Y. Analysis and Design of High-Efficiency Bidirectional GaN-based CLLC Resonant Converter. *Energies* **2019**, *12*, 3859. [CrossRef]
- de Oliveira, E.F.; Zacharias, P. Comprehensive Mode Analysis and Optimal Design Methodology of a Bidirectional CLLC Resonant Converter for E-Vehicles Applications. In Proceedings of the 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Genova, Italy, 3–5 September 2019; pp. 1–10. [CrossRef]
- 12. Zhao, L.; Pei, Y.; Wang, L.; Pei, L.; Cao, W.; Gan, Y. Design Methodology of Bidirectional Resonant CLLC Charger for Wide Voltage Range Based on Parameter Equivalent and Time Domain Model. *IEEE Trans. Power Electron.* **2022**, 1. [CrossRef]
- Min, J.; Ordonez, M. Bidirectional Resonant CLLC Charger for Wide Battery Voltage Range: Asymmetric Parameters Methodology. IEEE Trans. Power Electron. 2021, 36, 6662–6673. [CrossRef]
- 14. Zhang, C.; Li, P.; Kan, Z.; Chai, X.; Guo, X. Integrated Half-Bridge CLLC Bidirectional Converter for Energy Storage Systems. *IEEE Trans. Ind. Electron.* **2018**, *65*, 3879–3889. [CrossRef]
- 15. Lin, F.; Zhang, X.; Li, X. Design Methodology for Symmetric CLLC Resonant DC Transformer Considering Voltage Conversion Ratio, System Stability, and Efficiency. *IEEE Trans. Power Electron.* **2021**, *36*, 10157–10170. [CrossRef]
- Siebke, K.; Mallwitz, R. Operation Mode Analysis of the CLLC Resonant Converter. In Proceedings of the 2019 IEEE 13th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Sonderborg, Denmark, 23–25 April 2019; pp. 1–6. [CrossRef]
- Li, X.; Huang, J.; Ma, Y.; Wang, X.; Yang, J.; Wu, X. Unified Modeling, Analysis, and Design of Isolated Bidirectional CLLC Resonant DC–DC Converters. *IEEE J. Emerg. Sel. Top. Power Electron.* 2022, 10, 2305–2318. [CrossRef]
- Li, R.; Shi, F.; Cai, X.; Xu, H. Influence of Parasitic Parameters on DC–DC Converters and Their Method of Suppression in High Frequency Link 35 kV PV Systems. *Energies* 2019, 12, 3743. [CrossRef]
- Zhang, W.; Wang, F.; Costinett, D.J.; Tolbert, L.M.; Blalock, B.J. Investigation of Gallium Nitride Devices in High-Frequency LLC Resonant Converters. *IEEE Trans. Power Electron.* 2017, 32, 571–583. [CrossRef]
- SkyWorks Inc. Drivers SI 827x-Datasheet. Available online: https://www.skyworksinc.com/-/media/SkyWorks/SL/ documents/public/data-sheets/Si827x.pdf (accessed on 19 September 2022).
- 21. Sullivan, C.R.. Optimal choice for number of strands in a litz-wire transformer winding. *IEEE Trans. Power Electron.* **1999**, 14, 283–291. [CrossRef]
- 22. Sullivan, C.R.; Zhang, R.Y. Simplified design method for litz wire. In Proceedings of the 2014 IEEE Applied Power Electronics Conference and Exposition—APEC 2014, Fort Worth, TX, USA, 16–20 March 2014; pp. 2667–2674. [CrossRef]
- Rossmanith, H.; Stenglein, E. Prediction of the leakage inductance in high frequency transformers. In Proceedings of the 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), Karlsruhe, Germany, 5–9 September, 2016, pp. 1–10. [CrossRef]
- 24. Ouyang, Z.; Zhang, J.; Hurley, W.G. Calculation of Leakage Inductance for High-Frequency Transformers. *IEEE Trans. Power Electron.* 2015, *30*, 5769–5775. [CrossRef]
- 25. McLyman, C.W.T. Transformer and Inductor Design Handbook; CRC Press: Idyllwild, CA, USA, 2004.
- GaN System. GS66508T Top-Side Cooled E-Mode GaN Transistor-Datasheet. Available online: https://gansystems.com/gantransistors/gs66508t/ (accessed on 19 September 2022).
- Ferroxcube.pl. RM Cores and Accessories-Datasheet. Available online: https://ferroxcube.home.pl/prod/assets/rm12i.pdf (accessed on 19 September 2022).
- TDK, Ferrite N97-Datasheet. Available online: https://www.tdk-electronics.tdk.com/download/528886/cf0d9784d3d2438b5 2ade72fbb86ecf6/pdf-n97.pdf (accessed on 19 July 2021).
- Hua, W.; Wu, H.; Yu, Z.; Xing, Y.; Sun, K. A Phase-Shift Modulation Strategy for a Bidirectional CLLC Resonant Converter. In Proceedings of the 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019-ECCE Asia), Busan, Republic of Korea, 27–30 May 2019; pp. 1–6. [CrossRef]
- Ammar, A.M.; Ali, K.; Rogers, D.J. Converter for Plug-In Electric Vehicles On-Board Chargers. In Proceedings of the IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society, Singapore, 18–21 October 2020; pp. 1129–1135. [CrossRef]

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