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Review

Bandpass Sigma–Delta Modulation: The Path toward RF-to-Digital Conversion in Software-Defined Radio

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Abstract: This paper reviews the state of the art on bandpass ΣΔ modulators (BP-ΣΔMs) intended to digitize radio frequency (RF) signals. A priori, this is the most direct way to implement software-defined radio (SDR) systems since the analog/digital interface is placed closer to the antenna, thus reducing the analog circuitry and doing most of the signal processing in the digital domain. In spite of their higher programmability and scalability, RF BP-ΣΔM analog-to-digital converters (ADCs) require more energy to operate in the GHz range as compared with their low-pass (LP) counterparts. This makes conventional direct conversion receivers (DCRs) the commonplace approach due to their overall smaller energy consumption. This paper surveys some circuits and systems techniques which can make RF ADCs and SDR-based transceivers more efficient and feasible to be embedded in mobile terminals.

Keywords: analog-to-digital conversion; sigma–delta modulation; software-defined radio

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1. Introduction

The micro/nanoelectronics industry has exponentially grown over the last six decades according to Moore's law, yielding to the integration of dozen of billions of transistors with dimensions closer to a few atoms of silicon. Among other benefits, high levels of integration allow to embed more and more functionalities onto a single chip, including sensing interfaces, communication systems, memory and computing, among others. In addition to the reduced cost, technology downscaling has pervasively miniaturized the electronic devices, going from multi-chip components connected in printed circuit boards (PCBs) to *chip sets* encapsulated in system-in-packages (SiPs) to monolithic system-on-chip (SoC) solutions. This pervasive miniaturization is making it possible for electronic devices and their derived technologies—such as artificial intelligence (AI), big data, robotics, Internet of Things (IoT), etc.—to be more and more present in our daily lives [1–3]. These technologies are accelerating their pace of penetration, transforming many of our social and economic activities from a physical to virtual format. Indeed, our natural environment is being surrounded with a set of *digital layers*, which allows us to iterate with virtual entities and objects in an augmented reality—also referred to as the *metaverse* [4].

Communication systems are essential parts of IoT nodes and end terminals. In the majority of cases, information is transmitted wirelessly over radio frequency (RF) bands of the electromagnetic spectrum, i.e., carried out by analog signals. This requires an important portion of wireless transceivers to perform their functions in the analog/RF domain to adapt and transform signals from/to the digital domain, where they are processed by the digital signal processor (DSP). Unfortunately, analog components do not scale as digital parts do. Indeed, deep nanometer mainstream CMOS technologies are more suited to integrate fast digital transistors rather than accurate analog circuits. This is one of the main reasons why every time a new communication protocol is developed, it usually requires dedicated RF chip sets. As a consequence, the celerity with which new functionalities are incorporated in *i-devices* exceeds the rate of package reduction, and the trend from multi-chip to SiPs and SoCs

is still a technological challenge in reaching the requested quality standards while keeping the form factor, cost and time-to-market deployment reduced [5–10].

Addressing this challenge implies redefining the concept of mobile terminals, going from pure hardware-based to hybrid hardware/software-based devices. As envisaged by Mitola in 1995 [11], a software-defined radio (SDR) is defined as a universal radio platform which can be programmed to steer any frequency band, and process arbitrary communication protocols, while ensuring the required quality of service as well as guaranteeing privacy and security [6]. An ideal SDR transceiver—conceptually depicted in Figure 1a—would process all information in the digital domain so that it would be composed by three main building blocks: the antenna, the A/D interfaces and the DSP. This way, most parts of the hardware in this ideal SDR system are digital, thus benefiting from technology downscaling and a higher programmability to new standards and applications. Unfortunately, this implementation is not realistic due to the huge amount of power consumed by the A/D interfaces—the analog-to-digital converter (ADC) in the receiver and the digital-to-analog converter (DAC) in the transmitter—which requires at least some analog/RF signal conditioning circuitry to implement an efficient interface between RF signals and the digital data, depicted in Figure 1b.

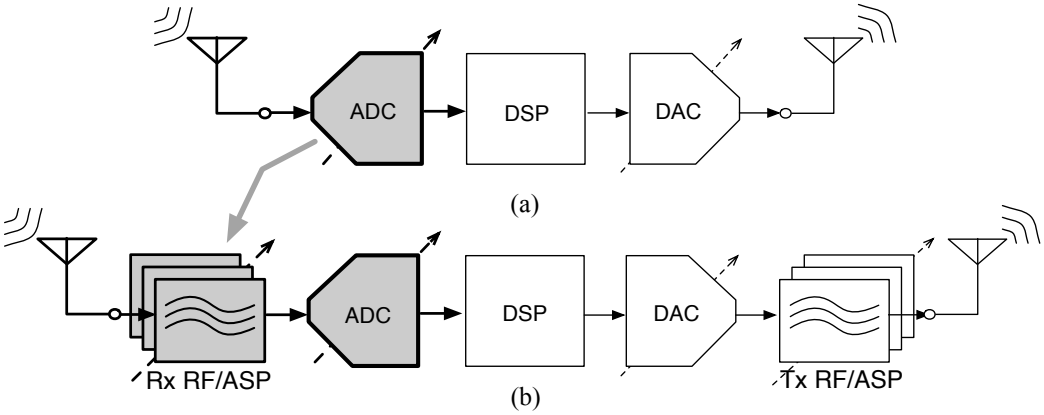

Figure 1. Software-defined radio transceiver. (**a**) Ideal concept. (**b**) Including RF/ASP interface.

The analog/RF-to-digital interface of multi-mode/multi-standard SDR transceivers can be implemented in two ways as depicted in Figure 2. In both cases, all building blocks need to be reconfigurable/programmable in order to adapt their performance to the required specifications. The approach in Figure 2a, known as direct conversion transceiver (DCT), translates the analog/RF signal from/to the RF domain to the baseband by means of an analog downconverter (in the receiver side) and an upconverter (in the transmitter side). This way, an LP ADC can be used to digitize downconverted signals in the receiver. Analogously, an LP DAC transforms the baseband digital data before being upconverted to RF in the transmitter. By contrast, the approach in Figure 2b requires to implement the analog/digital interfaces in the RF domain, i.e., an RF ADC in the receiver and an RF DAC in the transmitter. The main benefit of this approach is the reduced analog content, and hence, it is less sensitive to analog circuit impairments due to I/Q down-mixing, flicker noise and DC offset. However, the price to pay is that the RF/digital interface requirements are more demanding, with the subsequent penalty in the power consumption—a key factor in wireless transceivers and portable devices [12–16].

This paper focuses on the receiver path of SDR transceivers, considering the RF-digitization approach in Figure 2b and the ADC as one of its key building blocks. Target specifications for such an RF ADC may involve digitizing signals with an 8–12 bit effective resolution within a programmable 30 kHz–300 MHz bandwidth with a tunable carrier frequency ranging from 0.4 GHz to 6 GHz. These specifications should be fulfilled with a reduced amount of power to maximize device autonomy. Moreover, a high degree of programmability is needed in order to adapt the ADC performance to the electromagnetic

environment conditions, band occupancy, number of interferences, battery status, etc. The state of the art on ADCs for wireless communications is dominated by three techniques or a combination of them, namely: Sigma–Delta modulators (ΣΔMs), noise-shaping (NS) SAR and Pipeline. Although wideband Nyquist-rate ADCs—such as SAR, Pipeline or hybrid SAR-Pipeline—are potentially more efficient than ΣΔMs for digitizing wideband signals, bandpass (BP) ΣΔMs are, a priori, a better choice for implementing an early RF digitization of the desired signal band/channel in Figure 2b, with a high degree of tunability and adaptability of its performance metrics [17].

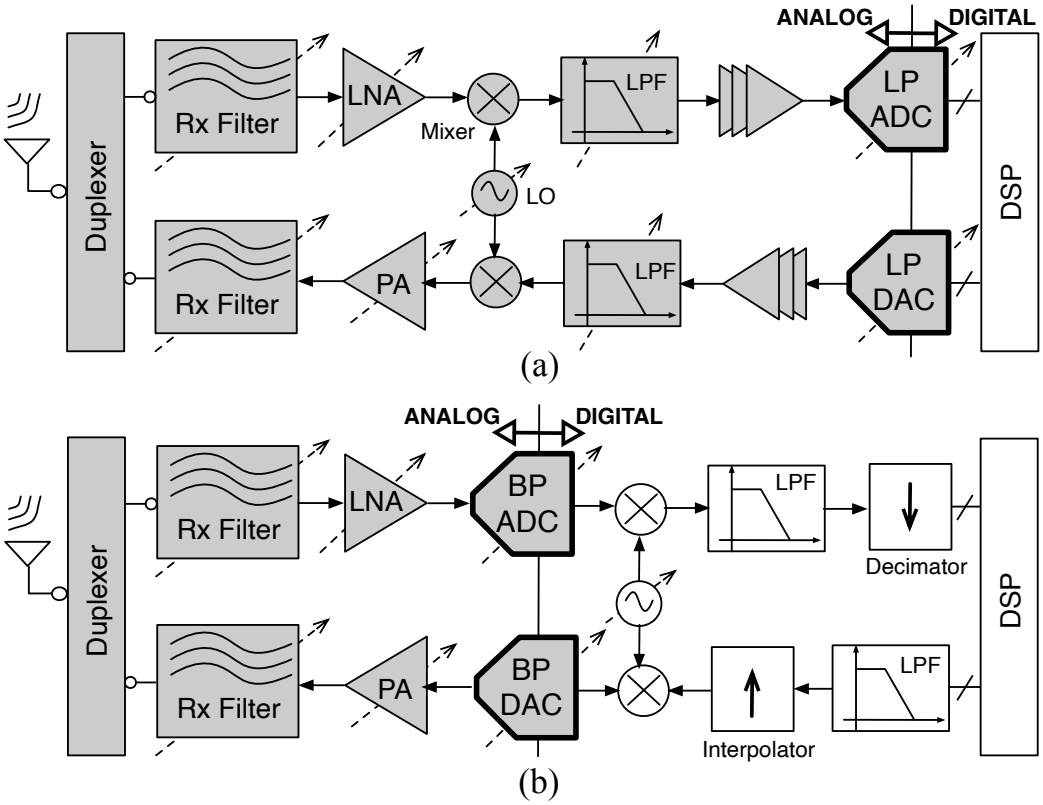

Figure 2. Conceptual diagram of reconfigurable RF transceivers based on the following: (**a**) Downconversion to baseband. (**b**) RF-Digitization (quadrature mixers, not drawn for simplicity, are assumed).

Since their conception in 1989 [18,19], a number of BP-ΣΔM ADCs have been reported to implement RF digitizers [16,20–36]. In spite of the promise of being the best solution for RF-to-digital conversion, performance metrics of BP-ΣΔMs are less efficient than their low-pass (LP) counterparts. The reasons behind this will be analyzed in this paper through a review of the state of the art. The main BP-ΣΔM architectures and circuit techniques will be overviewed and compared in terms of their main performance metrics, namely, effective resolution, operating frequency, and power dissipation. Cutting-edge circuits and systems will be identified to help designers select the most suited BP-ΣΔM topology and circuit technique according to their target specifications.

Following this introduction, the paper is organized as follows. Section 2 revisits the fundamentals and basic concepts of BP-ΣΔMs, putting emphasis on the discrete-time (DT) implementations. Section 3 overviews continuous-time (CT) BP-ΣΔMs, focusing on their use in RF ADCs in SDR receivers. Section 4 analyzes the state of the art on BP-ΣΔMs and compares their performance metrics with ΣΔMs and other kinds of ADCs. Emerging circuits and systems techniques are identified as potential *game changers* to digitize RF signals in SDR systems. Finally, conclusions are drawn in Section 5.

2. Bandpass ΣΔ Modulators: Fundamentals and Basic Concepts

Figure 3 shows the conceptual block diagram of a ΣΔM, which consists of a loop filter and a B-bit quantizer connected in a feedback loop [37]. Assuming a linear additive white noise model for the quantizer as depicted in Figure 3, the Z-transform of the ΣΔM output, y, can be written as follows.

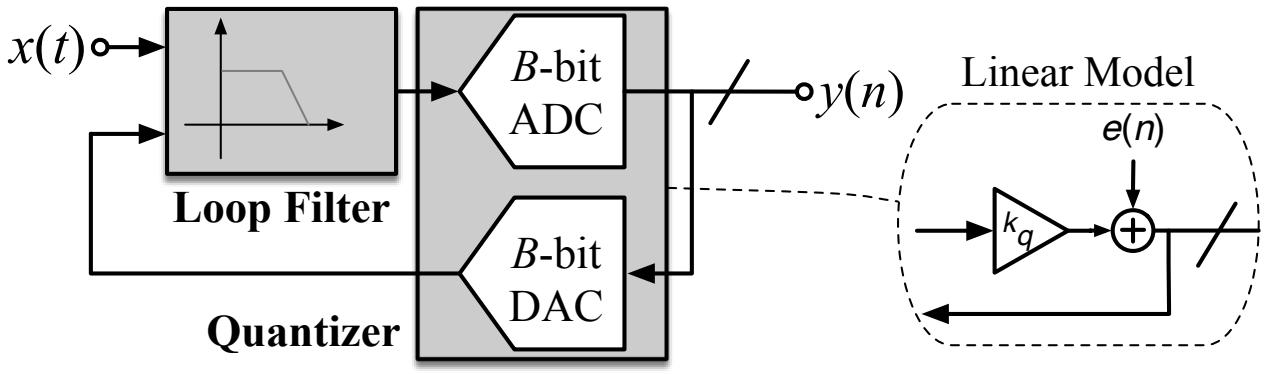

Figure 3. Conceptual block diagram of a ΣΔM.

$$Y(z) = \mathrm{STF}(z) \cdot X(z) + \mathrm{NTF}(z) \cdot E(z) \tag{1}$$

where STF and NTF stand for the signal- and noise-transfer functions, respectively, given by

$$\mathrm{STF}(z) = \frac{k_q \cdot H(z)}{1 + k_q \cdot H(z)}, \ \mathrm{NTF}(z) = \frac{1}{1 + k_q \cdot H(z)} \tag{2}$$

with k_q being the gain of the quantizer and $H(z)$ being the transfer function of the loop filter. Considering an Lth-order loop filter, the dynamic range (DR) of a ΣΔM can be approximately written as

$$\mathrm{DR} \approx 6.02 \cdot B + 1.76\mathrm{dB} + 10 \log_{10}[(2L+1) \cdot \mathrm{OSR}^{(2L+1)} / \pi^{2L}] \tag{3}$$

where $\mathrm{OSR} \equiv f_s / (2 \cdot B_w)$ stands for the *oversampling ratio*, f_s is the sampling frequency, and B_w is the signal bandwidth. The effective number of bits (ENOB) of a ΣΔM can be obtained from Equation (3) as

$$\mathrm{ENOB\ (bit)} = \frac{\mathrm{DR\ (dB)} - 1.76}{6.02} \tag{4}$$

Hence, ΣΔMs increase ENOB with OSR by approximately $3(2L+1)$ dB/octave—second term in (3). The three *key parameters*, namely OSR, L and B, define the system-level performance of ΣΔMs, and can be combined in many ways, giving rise to a huge number of ΣΔMs—LP or BP; single-loop or cascade; single-bit or multi-bit; continuous-time (CT) or switched-capacitor (SC)—in order to achieve the maximum DR. In the case of BP-ΣΔMs—the object of this paper—the zeroes of the NTF are placed around an arbitrary frequency, usually referred to as the *notch frequency*, f_n. This frequency corresponds to the carrier frequency of incoming signals in RF receivers as illustrated in Figure 4. The quantization noise is reduced only in a narrow band (B_w) around f_n, thus taking advantage of a high OSR to meet the required DR according to Equation (3) [37].

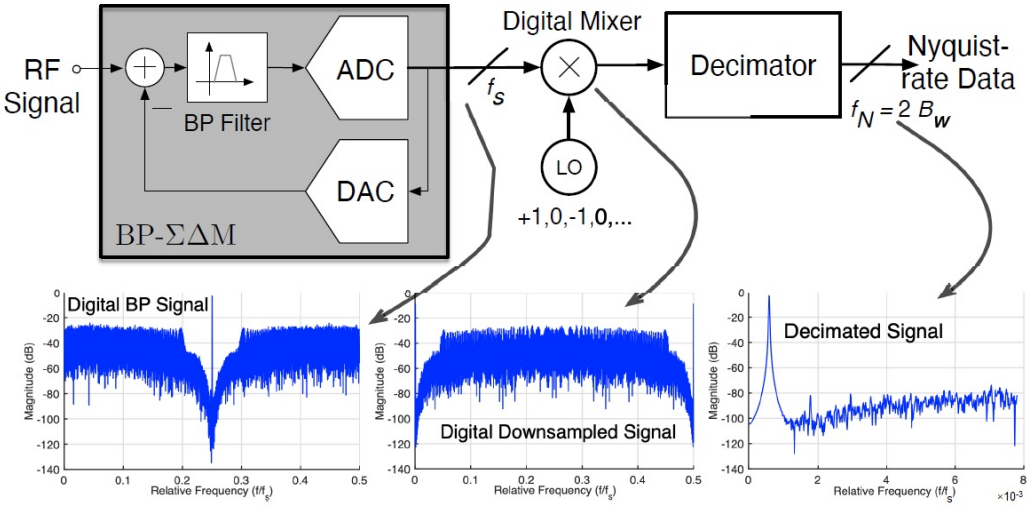

Figure 4. Illustrating the signal processing in a RF Rx based on BP-ΣΔMs with $f_n = f_s/4$.

2.1. Quantization Noise Shaping in BP-ΣΔMs

BP-ΣΔMs can be implemented using either discrete-time (DT)—basically switched capacitor (SC)—or CT circuit techniques. The latter are mostly used in RF ADCs due to their higher operating frequencies—in the GHz range. Moreover, CT circuits merge better with other circuits of the SDR receiver and implement some RF functions, such as out-of-band blocker, image-rejection filtering, anti-aliasing, etc. [38]. However, as will be discussed later in this paper, CT BP-ΣΔMs are usually synthesized from their equivalent DT counterparts. In the analysis that follows, a DT realization is assumed without loss of generality.

In the more general case, the loop-filter of BP-ΣΔMs is a 2*Lth*-order BP filter composed of *LC resonators*—or *biquad* sections—with a transfer function given by [39]:

$$H_R(z) = \frac{N(z)}{(1 - z^{-1} \cdot z_n) \cdot (1 - z^{-1} \cdot z_n^*)} \tag{5}$$

where $N(z)$ denotes the numerator polynomial and z_n and z_n^* stand for conjugate-complex poles of $H(z)$. Replacing Equation (5) in Equation (2) and assuming $k_q = 1$, it can be shown that the NTF of BP-ΣΔMs can be expressed as

$$\mathrm{NTF}(z) = \frac{[(1 - z^{-1} \cdot z_n) \cdot (1 - z^{-1} \cdot z_n^*)]^L}{[N(z) + (1 - z^{-1} \cdot z_n) \cdot (1 - z^{-1} \cdot z_n^*)]^L} \tag{6}$$

which has L zeros placed at $z = z_n$ and $z = z_n^*$. Assuming that $z_n = e^{j \cdot (2 \cdot \pi \cdot f_n \cdot T_s)}$, with $T_s = 1/f_s$ being the sampling period, and considering that $N(z)$ is designed so that the denominator in Equation (6) is unity, the NTF of an 2*Lth*-order BP-ΣΔM can be written as

$$\mathrm{NTF}(z) = [1 - 2 \cdot \cos(2\pi \cdot f_n \cdot T_s) \cdot z^{-1} + z^{-2}]^L \tag{7}$$

Note that NTF has its zeroes placed on the Z-domain unit circle at complex-conjugate z_n and z_n^*, i.e., $f = f_n$ and $f = -f_n$. This means that a 2Lth-order BP-ΣΔM has L zeroes placed at the signal band, thus being equivalent to an Lth-order LP-ΣΔM. As illustrated in the simulations shown in Figure 5, the notch frequency, f_n, can be programmed in order to make BP-ΣΔMs tunable within the Nyquist band, i.e., from DC to $f_s/2$. As will be discussed later, this feature is applied in wireless transceivers to increase the programmability of RF digitizers by reducing the quantization noise around the desired signal channel.

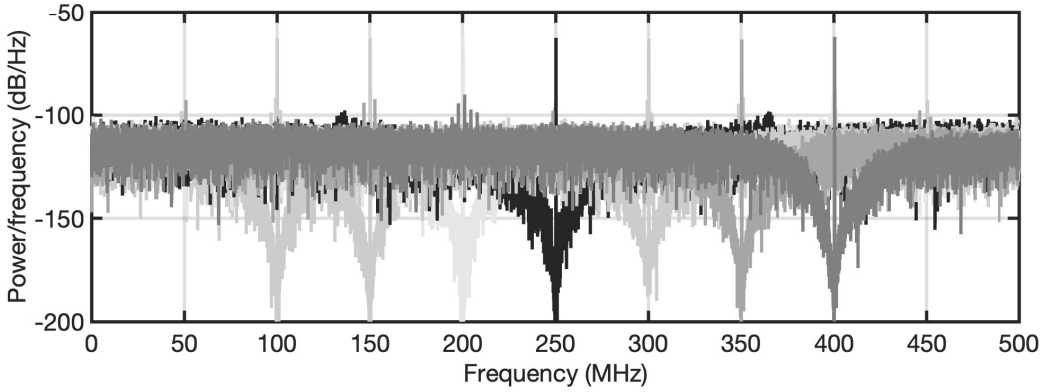

Figure 5. Noise-shaping programmability in BP-ΣΔMs from $f_n = 0.1 \cdot f_s$ to $f_n = 0.4 \cdot f_s$ ($f_s = 1$ GHz).

The power spectral density (PSD) of the quantization noise shaped by BP-ΣΔMs can be calculated as

$$\mathrm{PSD}_Q(f) = \frac{\Delta^2}{12 f_s} \cdot |\mathrm{NTF}(f)|^2 = \frac{\Delta^2}{12 f_s} \cdot |4 \cdot \sin[\pi \cdot (f - f_n) \cdot T_s] \cdot \sin[\pi \cdot (f + f_n)]|^{2L} \quad (8)$$

where Δ is the quantization step, defined as $\Delta \equiv X_{\mathrm{FS}}/(2^B - 1)$, with X_{FS} being the full-scale (FS) range of the quantizer.

The quantization in-band noise power, P_Q, can be computed by integrating $\mathrm{PSD}_Q(f)$ in the signal bandwidth as

$$P_Q = 2 \cdot \int_{f_n - B_w/2}^{f_n + B_w/2} \mathrm{PSD}_Q(f) \mathrm{d}f \approx \frac{\Delta^2}{12} \frac{[\pi \cdot \sin(2\pi \cdot f_n \cdot T_s)]^{2L}}{(2L+1)\mathrm{OSR}^{(2L+1)}} \quad (9)$$

Knowing that $\mathrm{DR}|_{\mathrm{dB}} = 10\log[(X_{\mathrm{FS}}/2)^2/(2 \cdot P_Q)]$, it can be shown that in the case of BP-ΣΔMs, DR is given by [39]

$$\mathrm{DR}|_{\mathrm{BP}} \approx 6.02 \cdot B + 1.76\mathrm{dB} + 10\log_{10}[(2L+1) \cdot \mathrm{OSR}^{(2L+1)}/[\pi \cdot \sin(2\pi \cdot f_n \cdot T_s)]^{2L}] \quad (10)$$

Note that the above expression is equal to (3) if $f_n = f_s/4$. This notch location is the most common case as discussed below.

2.2. Notch Frequency Location and Basic Architectures

One of the most common choices for the notch frequency is $f_n = f_s/4$ since this passband location optimizes the trade-off between anti-aliasing filtering and image-rejection filtering in wireless transceivers based on BP-ΣΔMs as that shown in Figure 2 [39]. The digital downconverter in Figure 2 can be notably simplified since the (digital) local oscillator (LO) signal is designed such that it generates a digital sinewave as

$$\sin(2\pi \cdot f_n \cdot n \cdot T_s)|_{f_n = f_s/4} = \sin(n \cdot \pi/2) = \mathbf{[1,0,-1,0]}, 1, 0, -1, 0... \quad (11)$$

which is a data series of $+1$ s, 0 s, and -1 s, easily implemented by simple digital logic. This makes it easier and simple the gate-level implementation of the digital mixer and the numerical controlled oscillator (NCO) in Figure 2. More importantly, assuming $f_n = f_s/4$ in (7), the NTF of a $2L$-th order BP-ΣΔM yields

$$\mathrm{NTF}(z)|_{(f_n = f_s/4)} = [1 + z^{-2}]^L \quad (12)$$

which can be derived by applying a $z \to -z^2$ transformation to the NTF of a Lth-order low-pass (LP) ΣΔM, given by $(1 - z^{-1})^L$ [37]. This way, any arbitrary BP-ΣΔM can be derived from an initial LP-ΣΔM by applying this Z-domain transformation. Figure 6 illustrates this

transformation applied to a 2nd-order LP-ΣΔM, which becomes a 4th-order BP-ΣΔM, and loop-filter integrators are transformed into resonators.

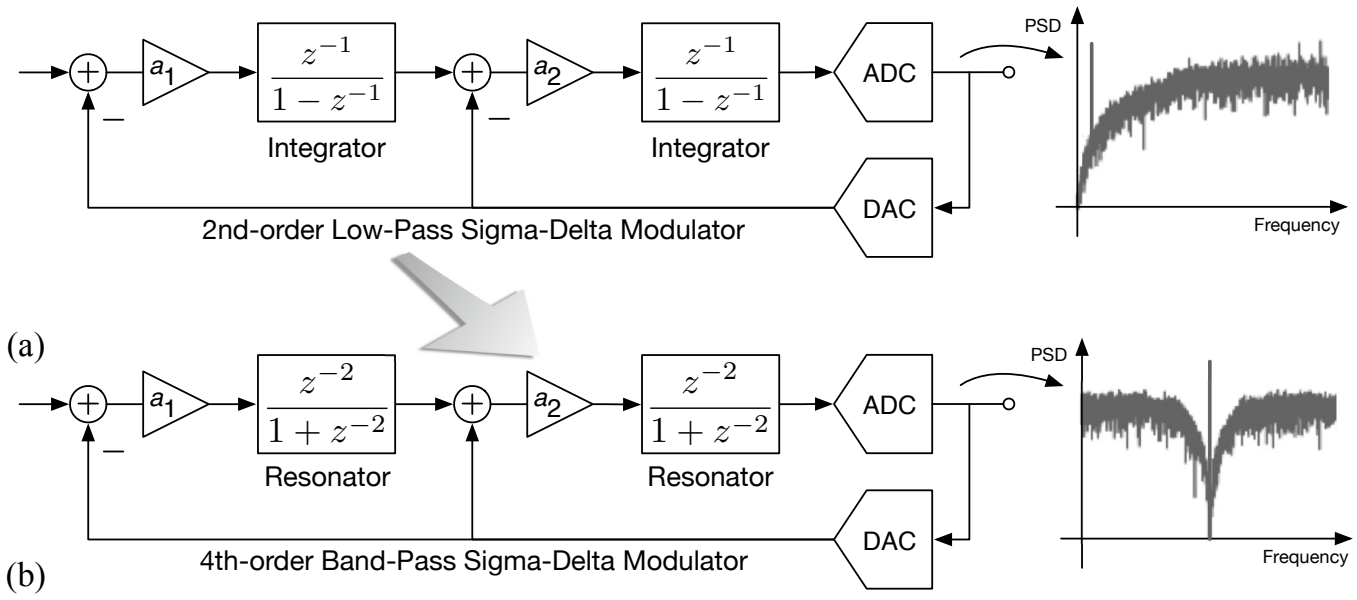

Figure 6. LP-to-BP $z \rightarrow -z^2$ transformation: (**a**) 2nd-order LP-ΣΔM, (**b**) 4th-order BP-ΣΔM.

The $z \rightarrow -z^2$ transformation also allows to place the input signal at $3f_s/4$ [40] instead of $f_s/4$ given that the spectrum is symmetrical with respect to $f_s/2$. Making $f_{\mathrm{IF}} = 3f_s/4$ preserves the requirements of the anti-aliasing filter compared to the $f_{\mathrm{IF}} = f_s/4$ case, but the image-rejection filter specifications can be relaxed. In addition, it allows for either the clock rate to be reduced to $1/3$ or the signal processing to be three times faster. However, the OSR is also reduced by a factor of three with the subsequent penalty in DR loss.

Placing the signal band around $f_s/4$ also has some disadvantages. On the one hand, in the presence of nonlinearities of the analog circuitry of the ΣΔM, any intermodulation distortion products resulting from the mixing of tones at $f_s/2$ with the input signal will fall inside the modulator passband and will thus corrupt the signal information. On the other, for a given RF input, the clock rate demands are more restrictive than placing f_n between $f_s/4$ and $f_s/2$. For instance, those wireless standards—such as some IEEE 802.11 standard—operating in the frequency band of 5 GHz would require a sampling frequency of 20 GHz, with the subsequent penalty in power dissipation [41].

Although placing the notch frequency at $f_s/4$ is the most common approach, other alternative approaches have been reported to synthesize BP-ΣΔMs and allocate the zeroes of the NTF. Some techniques are based on the use of *complex* BP filters in *quadrature* architectures [42,43] as illustrated in Figure 7a. The resulting NTF has complex zeroes that are not necessarily conditioned to be placed symmetrically around DC. This allows an L-th order BP-ΣΔ to place L zeroes at f_n without having any zero at $-f_n$. The solution is more energy efficient than conventional approaches since no power is dedicated to digitizing the negative (imaginary) frequency bands [44]. One of the main limitations of this approach is the mismatch between both real and imaginary paths, which causes signal image components to appear in the signal band, thus corrupting the information. This problem can be mitigated by placing some zeroes in the imaginary band—as illustrated in Figure 7b. However, this reduces the ratio between the number of NTF zeroes and the filter order—one of the main benefits of quadrature BP-ΣΔMs.

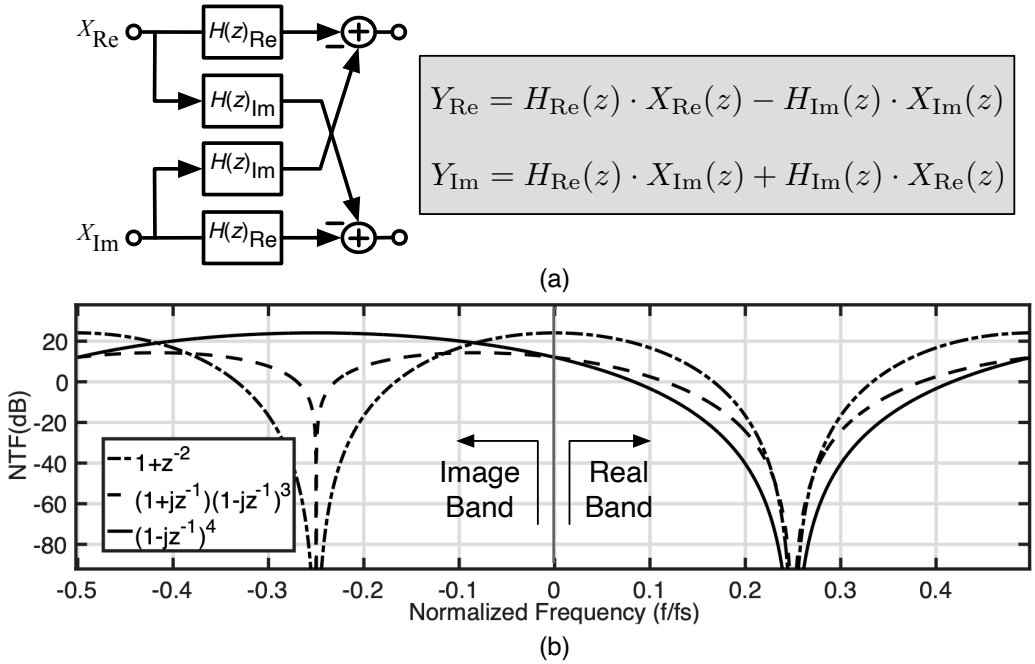

Figure 7. Quadrature BP-ΣΔMs. (**a**) Block diagram of a complex BP filter. (**b**) NTF with asymmetric placement of zeroes.

Another alternative to reduce the clock rate as compared to the $f_n = f_s/4$ approach is based on time-interleaved (TI) or P-path loop filters [45]. The idea of TI BP-ΣΔM consists of splitting a modulator clocked at f_s in several TI BP-ΣΔM paths, each one operating at f_s/P, with P being the number of paths, as illustrated in Figure 8. Similar to quadrature BP-ΣΔMs, TI BP-ΣΔMs are also limited by circuit impairments, such as offset, gain and timing mismatch, which causes spur tones to appear at the output spectrum, thus degrading the noise shaping [46].

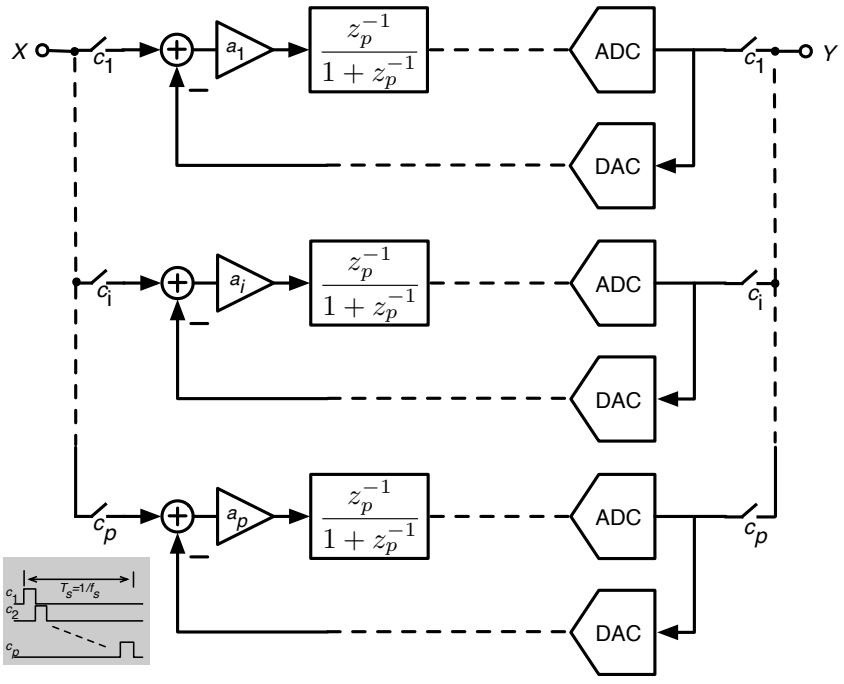

Figure 8. Conceptual block diagram of a TI BP-ΣΔM.

Based on a similar idea, some authors proposed a *polyphase* decomposition of the NTF of BP-ΣΔMs [47] as follows:

$$\mathrm{NTF_{PF}} = \sum_{0}^{P-1} z^{-j} \cdot N_j(z^P) \tag{13}$$

where $N_j(z^P)$ stands for transfer functions of the j-th path BP-ΣΔM. For instance, let us assume a 2nd-order polyphase BP-ΣΔM with $P = 2$ and a NTF with zeros at $z = e^{\pm j\alpha}$, given by

$$\mathrm{NTF_{PF2}} = 1 + \beta z^{-1} + z^{-2} \tag{14}$$

In this case, the polyphase ($P = 2$) decomposition leads to $N_0(z^{-2}) = 1 + z^{-2}$ and $N_1(z^{-2}) = \beta$, where β is a coefficient that changes the zeroes of NTF from $z = 1$ to $z = -1$, when it varies from $\beta = -2$ to $\beta = 2$. Assuming that $\beta = -2 \cdot \cos(2\pi \cdot f_n \cdot T_s)$, we obtain the expression of NTF given in Equation (7). It can be shown that the spur tones due to path mismatches fall out of the signal band at f_s/P, with P being the number of paths used in the polyphase decomposition [47].

3. Continuous-Time BP-ΣΔMs

The BP-ΣΔMs described above assume a DT (usually SC) realization of the loop filter. However, CT BP-ΣΔMs are more suited to digitize RF signals since GHz-range sampling rates are needed. CT loop filters can operate at higher frequencies than their SC counterparts, while consuming less power and implement an inherent anti-aliasing filtering. The loop-filter of CT BP-ΣΔMs can be realized using either active (RC or Gm-C) resonators or passive LC resonators as conceptually depicted in Figure 9. RF BP-ΣΔMs have two main design challenges. The first is to achieve a high-quality and accurate resonance frequency. The second is to target a wide tuning range of the carrier (or *notch*) frequency. LC tanks are a good approach from a power and linearity perspective, although they typically support only an octave of range, whereas active-(Gm-C/RC) resonators can be widely tunable but require amplifiers with strong requirements—high DC gain and gain bandwidth (GB) [48]. Single op amp resonators are a good alternative to reduce power consumption. Some authors propose the use of positive feedback—implemented by a passive RC network—to enhance the quality factor of resonators. Figure 9d illustrates this approach proposed by Chae et al. [49].

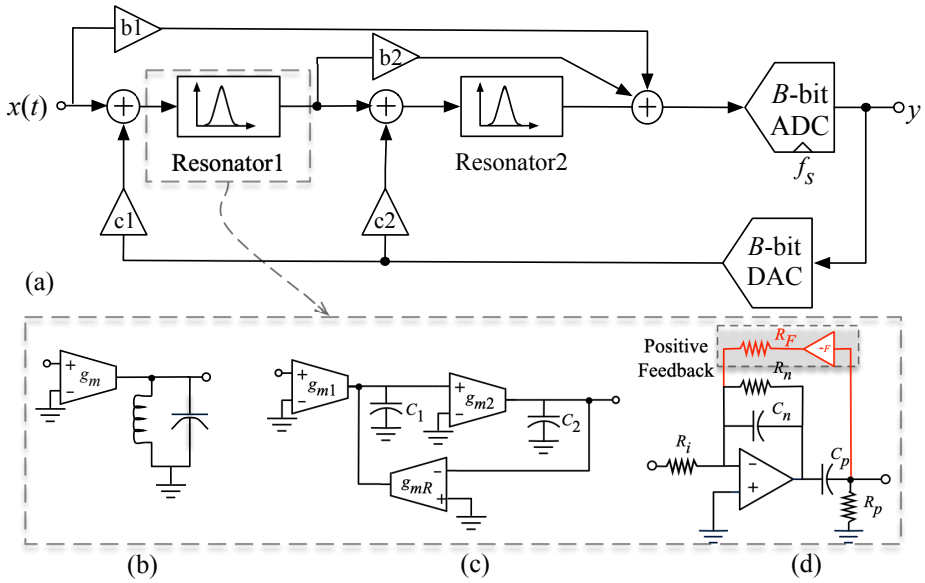

Figure 9. (**a**) Conceptual diagram of BP CT-ΣΔMs based on (**b**) LC-tank resonators, (**c**) active Gm-C integrators, and (**d**) single op amp resonators with Q-factor boosting [49].

Regardless of the circuit technique used to implement CT BP-ΣΔMs, it is difficult to keep the required specifications within a wide tuning range. For that reason, it is usual to set the notch frequency constant, usually located at $f_n = f_s/4$. For the analysis that follows, this approach will be considered and the problem of tuning f_n will be discussed later.

3.1. LC-Based CT BP-ΣΔM Architectures

Figure 10 shows the block diagram of the two common approaches to implement CT BP-ΣΔMs with multi-path feedback, based on ideal (LC) resonators with a transfer function, $R(s) = \omega_o s/(s^2 + \omega_o^2)$. Normalized values of s and ω_o are considered with respect to f_s so that $s = 2\pi f/f_s$ (with f standing for the frequency variable) and $\omega_o = 2\pi f_n/f_s$. A 4th-order loop filter made up of two resonators with $f_n = f_s/4$ is considered. The feedback loop is implemented in two main different ways. Figure 10a [50] uses two different DAC pulse shapes, return-to-zero (RZ) and half-delay return-to-zero (HRZ), while Figure 10b [51] includes a non-return-to-zero (NRZ) DAC with different delay for each path. For the sake of simplicity, the excess loop delay (ELD) compensation path is not considered. In both cases, multiple feedback paths with their scaling coefficients are required to increase the degrees of freedom in the synthesis process, correctly restoring NTF of the DT Z-domain counterpart.

The CT BP-ΣΔMs shown in Figure 10 can be synthesized as follows. The Schreier's toolbox [52] is used to obtain the NTF which satisfies the required specifications in terms of DR and B_w with an out-of-band gain (OBG) (usually 1.5), and the DT version of the loop filter transfer function can be easily derived as $H(z) = 1 - 1/NTF(z)$. The DT version of the loop-filter transfer function, $H(z)$, of the desired BP CT-ΣΔM is therefore derived from the well-known impulse-invariant transformation as

$$H(z) \equiv Z\{L^{-1}[H(s) \cdot H_{\mathrm{DAC}}(s)]\} \tag{15}$$

where $Z(\cdot)$ and $L(\cdot)$ denote the Z-transform and L-transform symbols, respectively, and $H_{\mathrm{DAC}}(s)$ is the transfer function of the DAC [37,53].

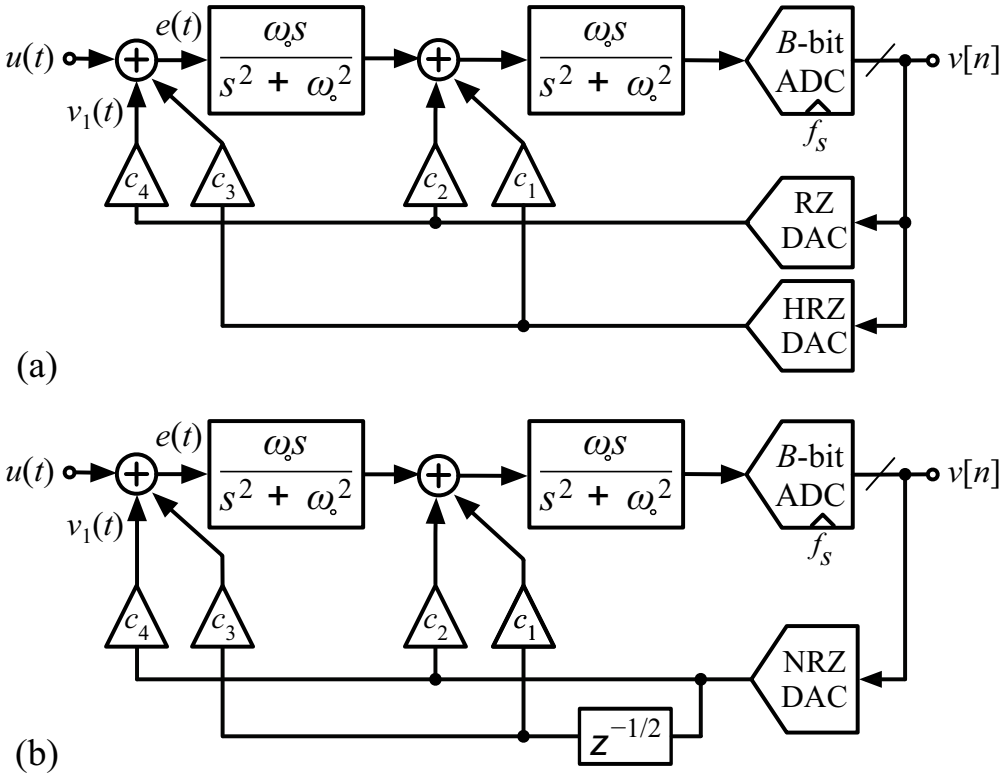

Figure 10. Conventional LC BP-ΣΔMs with a multi-path feedback loop based on the following: (**a**) Different DAC (RZ/HRZ) waveforms [50]. (**b**) Identical DAC (NRZ) with different delay [51].

3.2. Widely Tunable CT BP-ΣΔMs

As stated above, one of the challenges of RF ADCs is the high sampling frequency required. Using a fixed value of f_n (normally $f_n = f_s/4$), forces the variation of f_s in order to tune the desired carrier frequency of the RF signal. For instance, if the incoming RF signal is placed at $f_n = 5$ GHz, the sampling frequency should be $f_s = 4 \cdot f_n = 20$ GHz. Moreover, another important inconvenience of this approach is that a widely programmable PLL-based synthesizer is needed to vary f_s according to the f_n needed to place the in-coming RF signal within the passband of the modulator. For instance, if an RF ADC needs to digitize RF signals which are placed in the wireless commercial band, i.e., 0.4–6 GHz, this would require a PLL with a frequency tuning range from 1.6 GHz to 24 GHz!

These limitations have motivated the interest for programmable CT BP-ΣΔMs with tunable notch frequency [24,25]. In the majority of cases, tuning range of notch frequency is limited by stability of the modulator loop filter. This problem can be circumvented if the notch frequency is taken into account as a design parameter of the BP-ΣΔM. This approach, referred to as *notch-aware* systematic methodology [41], allows to increase the tunable notch-frequency range of LC-based BP-ΣΔMs with respect to prior art, ranging from $0.1f_s$ to $0.4f_s$, while keeping their performance in terms of noise shaping, stability and sensitivity to architecture- and circuit-level nonideal effects [41].

As an illustration, let us consider the Gm-LC BP-ΣΔM with 4-bit quantizer shown in Figure 11. This modulator was synthesized using the *notch-aware* synthesis methodology. First, the Schreier toolbox is used to obtain the DT version of the NTF. The next step consists of obtaining the open-loop transfer function—from the modulator output to the input of the quantizer, computed for the different feedback branches with gain c_i in Figure 10b as follows:

$$H_{c_i}(s,v) = c_i \cdot e^{-sp} \cdot \left[\frac{(\frac{\pi}{v})s}{s^2 + (\frac{\pi}{v})^2}\right]^{\lfloor \frac{i}{2} \rfloor} \cdot H_{\text{NRZ-DAC}}(s) \quad (16)$$
$$(p = 2 \text{ for } i = 1 \text{ and } p = 1 \text{ for } i = 0, 2, 3, 4, 5)$$

where $\lfloor \cdot \rfloor$ denotes the floor operator, $v \equiv f_s/(2f_n) = \pi/\omega$, and $H_{\text{NRZ-DAC}}(s)$ stands for the transfer function of the NRZ DAC, respectively given by

$$H_{\text{NRZ-DAC}}(s) = T_s \cdot \frac{1 - e^{s/2}}{s} \quad (17)$$

The resulted modulator loop filter can be implemented using Gm-LC resonators as shown in Figure 11a. This circuit implementation increases the programmability of the loop-filter coefficients, which are realized as switchable unitary transconductance elements, g_{mu} as illustrated in Figure 11b. It can be shown that the block diagrams in Figures 10b and 11 are equivalent, if the following relationships are satisfied:

$$\begin{aligned} &g_{m1,2} = k_{1,2} \cdot C \cdot \omega \cdot f_s, \;\; g_{m3} = k_3/R \\ &I_{c1,c1d} = (c_1, c_{1d}) \cdot g_{m1} \cdot V_{\text{FS}} \\ &I_{c2,c2d} = (c_2, c_{2d}) \cdot g_{m2} \cdot V_{\text{FS}}/s_{\text{r1}} \end{aligned} \quad (18)$$

where V_{FS} stands for the full-scale reference voltage, $k_{1,2} = k/s_{\text{r1,2}}$ and $k_3 = 1/(s_{\text{r1}} \cdot s_{\text{r2}})$ are scaling forward-path coefficients, and $s_{\text{r1,2}}$ are the weight coefficients which scale the resonator gain, $R_{\text{gain}} = \omega \cdot s$. This way, the notch frequency of the modulator can be tuned as illustrated in the simulated output spectra shown in Figure 11c.

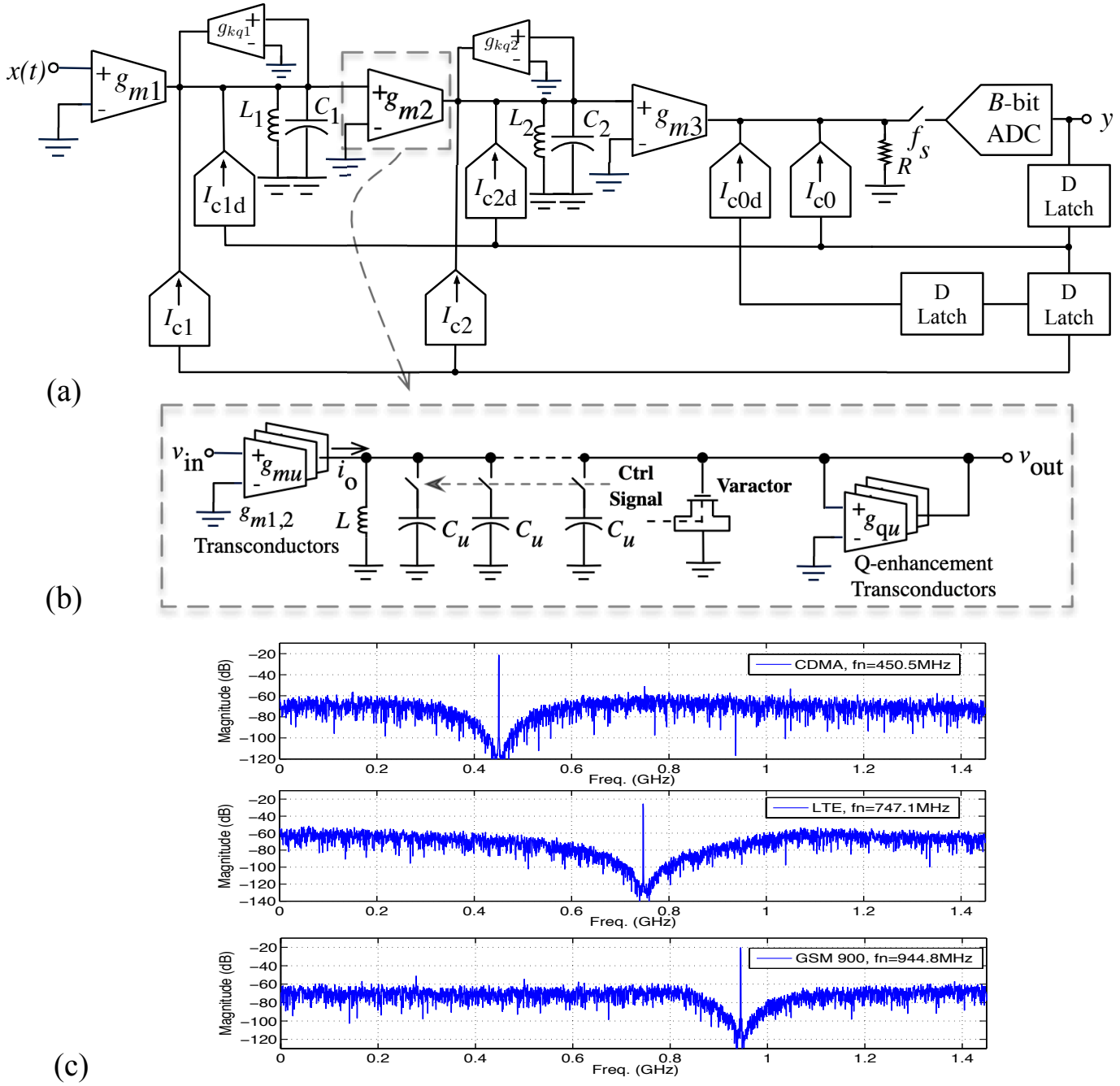

Figure 11. Tunable CT BP-ΣΔMs. (**a**) Block diagram, (**b**) Gm-LC resonator. (**c**) Output spectra [54].

4. State of the Art on BP-ΣΔMs

Since the first BP-ΣΔM was reported in the beginning of the 1990s [55], a vast number of integrated circuits (ICs) using diverse technologies, architectures and circuit techniques have been proposed [37]. The most important specifications of any ADC are the signal bandwidth, B_w, and the ENOB. In the case of BP-ΣΔMs, the notch frequency, f_n, should be also considered since it would affect the amount of energy (power) needed to digitize a signal placed on it. Tables 1 and 2 sum up the performance of the state-of-the-art BP-ΣΔM ICs considered in this survey. The data analyzed in this work are collected in a spreadsheet available at http://www.imse-cnm.csic.es/~jrosa/CMOS-SDMs-Survey-IMSE-JMdelaRosa_DEC2022.xlsx.

Table 1. Summary of the state of the art on SC BP-ΣΔM ICs (sorted by FOMS).

Ref.	DR (bit)	f_n (MHz)	B_w (MHz)	L	Tech./Sup.Volt	P (mW)	FOMS (dB)
[56]	6.8	10.7	0.2	2	0.35 mu/1 V	12.0	115
[57]	6.7	20.0	3.84	4	0.35 mu /3 V	56.0	120
[42]	10.8	3.75	0.2	4	0.8 mu/5 V	130.0	129
[58]	9.7	3.25	0.2	3	0.35 mu/3.3 V	18.7	130
[59]	9.0	2.0	0.03	4	2 mu/3.3 V	0.8	132
[60]	10.0	10.7	0.2	4	0.25 mu/1 V	8.5	136
[44]	12.0	10.7	0.2	6	0.35 mu/3.3 V	116.0	136
[57]	11.7	20.0	0.27	4	0.35 mu/3 V	56.0	139
[45]	12.2	20.0	0.2	4	0.6 mu/3.3 V	72.0	140
[61]	12.6	0.56	0.25	2-2	0.25 mu/2.5 V	77.0	143
[62]	11.7	3.25	0.2	4-2	0.8 mu/3 V	14.4	144
[60]	12.0	10.7	0.1	4	0.25 mu/1 V	8.5	145
[63]	12.0	16.0	2.0	6	0.25 mu/2.5 V	110.0	147
[60]	12.7	10.7	0.06	4	0.25 mu /1 V	8.5	147
[64]	11.7	20.0	1.76	4-4	0.35 mu/3 V	37.0	149
[65]	11.7	40.0	1.0	4	0.18 mu/1.8 V	16.0	150
[60]	13.4	10.7	0.06	4	0.25 mu/1 V	8.5	151
[66]	14.5	10.7	0.4	4	0.15 V/3.3 V	208.0	152
[66]	18.3	10.7	0.003	4	0.15 V/3.3 V	208.0	154
[66]	15.3	10.7	0.2	4	0.15 V/3.3 V	208.0	154
[67]	13.2	10.0	0.2	2	0.25 mu/2.1 V	10.0	154
[64]	13.3	20.0	1.25	4-4	0.35 mu/3 V	37.0	157
[68]	15.7	12.6	0.31	4	0.18 mu/1.8 V	115.0	160
[69]	14.4	40.0	2.5	4	0.18 mu/1.8 V	150.0	161

Table 2. Summary of the state of the art on CT BP-ΣΔMs (sorted by FOMS).

Ref.	DR (bit)	f_n (MHz)	B_w (MHz)	L	Tech./Sup.Volt	P (mW)	FOMS (dB)
[70]	6.0	1000	0.5	4	0.18 mu/1.8 V	290.0	61
[71]	7.2	100	0.2	4	0.35 mu/3.3 V	165.0	67
[72]	6.7	70	0.2	2	0.5 mu/2.5 V	39.0	68
[73]	8.9	225	100	6	65 nm/1 V	13.0	90
[74]	9.2	47.3	0.2	2	0.35 mu/3.3 V	45.0	90
[75]	8.0	2000	1.0	2	0.13 mu/1.2 V	30.0	92
[27]	6.8	2700	15.0	4	40 nm/1.1 V	90.0	103
[76]	10.8	10.7	0.2	6	0.5 mu /5 V	60.0	104
[74]	8.4	47.3	3.84	4	0.35 mu/3.3 V	45.0	109
[77]	6.3	2500	15.0	3	40 nm/1.1 V	90.0	109
[78]	8.1	4.09	4.0	2	0.25 mu /1.8 V	20.5	109
[78]	9.3	4.09	2.0	2	0.25 mu/1.8 V	20.5	114
[79]	9.3	228	4.0	4	65 nm/1 V	13.0	122
[80]	8.3	2440	28.0	4	0.13 mu/1.2 V	15.0	129
[81]	15.0	0.1	0.02	5	0.18 mu/2.9 V	9.1	130
[34]	7.0	3000	93.0	2	65 nm/1.2 V	13.0	130
[82]	13.3	10.7	0.2	5	0.25 mu/2.5 V	11.0	133
[83]	11.0	2.0	1.0	2	0.18 mu/1.8 V	2.2	134
[84]	14.0	10.7	0.5	5	0.18 mu/1.8 V	210.0	135
[85]	10.2	260	20.0	4	65 nm/1.4 V	124.0	135
[23]	7.7	2.2	80.0	4	40 nm/1.1 V	9.86	135
[86]	11.3	200	10.0	4	0.18 mu/1.8 V	160.0	137
[84]	19.3	10.7	0.003	5	0.18 mu/1.8 V	210.0	138
[32]	14.6	20.0	0.2	3	180 nm/1.8 V	25.8	142
[49]	9.7	200	24.0	4	65 nm/1.25 V	12.0	142
[87]	10.0	175	2.0	4	65 nm/1 V	0.15	144
[84]	16.0	10.7	0.2	5	0.18 mu/1.8 V	210.0	145
[81]	12.0	50.0	3.84	5	0.18 mu/ 2.9 V	14.1	146
[88]	8.3	1.5	300	4	28 nm/1 V	38.0	147
[20]	10.0	2.4	60.0	6	90 nm/1 V	40.0	148
[81]	13.5	50.0	1.23	5	0.18 mu/2.9 V	13.1	150
[28]	11.3	180	25.0	6	65 nm/1.2 V	35.0	152
[35]	9.8	100	30.0	2	28 nm/1 V	2.5	152
[89]	14.7	0.13	0.2	3	0.25 mu/1.8 V	2.7	152
[90]	11.3	200	25.0	6	65 nm/1 V	35.0	153
[91]	11.3	2.45	20.0	6	40 nm/1.1 V	20.0	153
[92]	12.0	6.0	10.0	2	65 nm/1.2 V	6.3	158
[93]	14.7	44.0	8.5	4	0.18 mu/2.9 V	375	163
[36]	11.2	400	100	2	28 nm/1 V	13.4	167

4.1. Low-Pass vs. Bandpass ΣΔMs

The analysis that follows focuses on BP-ΣΔMs, and hence, it is useful first to compare their performance with other types of ΣΔMs, generically grouped here as LP-ΣΔMs. Figure 12 represents the performance of cutting-edge ΣΔMs in terms of their main design specifications, i.e., the signal bandwidth, B_w and the resolution, characterized here by the ENOB. This plot—usually referred to as an *aperture plot*—shows also the state-of-the-art front, limited by the noise spectral density (NSD) given by

$$\text{NSD}|_{\text{dBFS/Hz}} \equiv (P_{\text{nd}}/B_w)|_{\text{dBFS/Hz}} \tag{19}$$

where P_{nd} is the noise-plus-distortion power referred to the full-scale (FS) range of the converter [48]. Note that the state-of-the-art front is dominated by LP-ΣΔMs, which approaches NSD $= -170$ dBFS/Hz, although there are some BP-ΣΔMs close to NSD $= -160$ dBFS/Hz, while digitizing signals with bandwidths over 100 MHz [36,88].

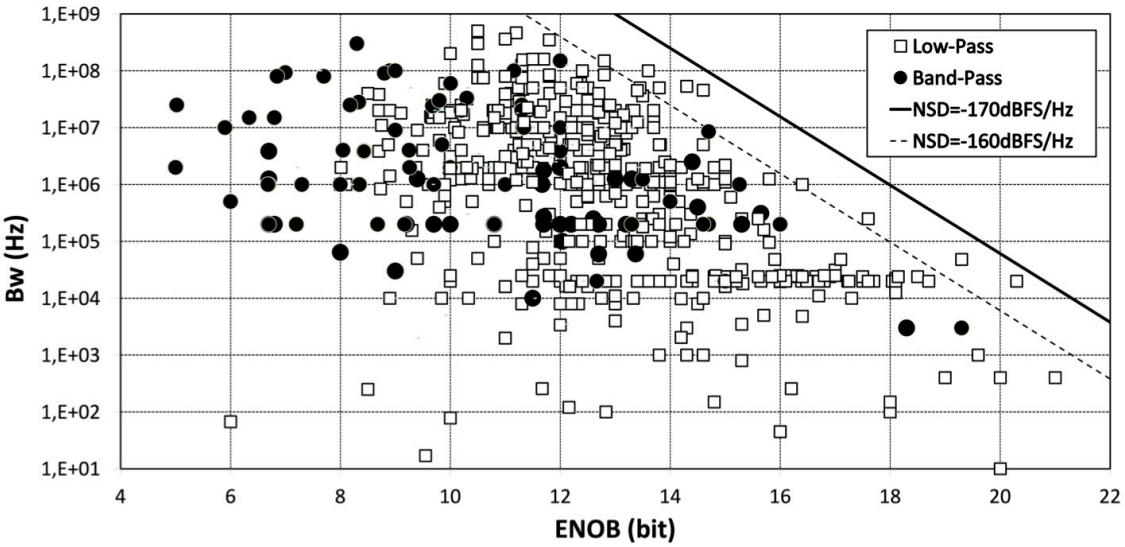

Figure 12. Aperture plot of ΣΔMs: BP-ΣΔMs vs. LP-ΣΔMs.

Apart from the main ADC specifications, ENOB and B_w, it is common to compare the efficiency of (ΣΔ) ADCs in terms of the amount of *energy* per converted sample—also referred to as *conversion energy*, E, defined as [94,95]

$$E \equiv \frac{P(\text{W})}{f_{\text{snyq}}(\text{Hz})} \tag{20}$$

where P stands for the power dissipated in Watts (W), and $f_{\text{snyq}} \equiv 2 \cdot B_w$, is the effective Nyquist rate, measured in samples per second (S/s). Figure 13 plots the *conversion energy* versus ENOB—also known as an *energy plot* [94,96]. This picture represents graphically the trade-off between resolution and conversion energy such that the larger the resolution, the more conversion energy is needed. It is therefore convenient to express this trade-off in a figure of merit (FOM), which takes into account the main performance metrics of an ADC, i.e., ENOB, B_w and P. The following two FOMs are the most used by the ADC designers community:

$$\begin{aligned} \text{FOMW} &\equiv \frac{E(\text{J})}{2^{\text{ENOB(bit)}}} \\ \text{FOMS} &\equiv \text{SNDR(dB)} + 10 \cdot \log_{10}[B_w(\text{Hz})/P(\text{W})] \end{aligned} \tag{21}$$

where SNDR is related to ENOB as SNDR(dB) $= 10 \cdot \log_{10}[(3/2) \cdot 4^{\text{ENOB(bit)}}] = 6.02 \cdot \text{ENOB(bit)} + 1.76$. FOMW, measured in J/conversion-step, was proposed by Walden [97], whereas FOMS is based on a FOM originally proposed by Rabii and Wooley [98], computed on a logarithmic scale, as suggested by Schreier and Temes in [99]. Note that FOMS can be also expressed in the following form:

$$\text{FOMS} \equiv P_{\text{sig}|_{\text{dBFS}}} - \text{NSD}|_{\text{dBFS/Hz}} - 10 \cdot \log_{10}[P(\text{W})] \tag{22}$$

where $P_{\text{sig}|_{\text{dBFS}}}$ denotes the input signal power computed in dB referred to the FS range of the converter. Therefore, the smaller the FOMW value and the larger the FOMS value, the "better" the ADC is. As a reference, FOMW and FOMS are also depicted in Figure 13, considering the following numerical values: FOMW =1 and 10 fJ/conv-step; FOMS = 175 dB and 185 dB. The resulted lines of constant FOMW and FOMS in Figure 13 can be respectively determined from Equation (21) as

$$\begin{aligned} E(\text{J})|_{\text{FOMW}} &= 2^{\text{ENOB(bit)}} \cdot \text{FOMW} \\ E(\text{J})|_{\text{FOMS}} &= \frac{3}{2} \cdot \frac{4^{\text{ENOB(bit)}}}{10^{\frac{\text{FOMS}}{10}}} \end{aligned} \tag{23}$$

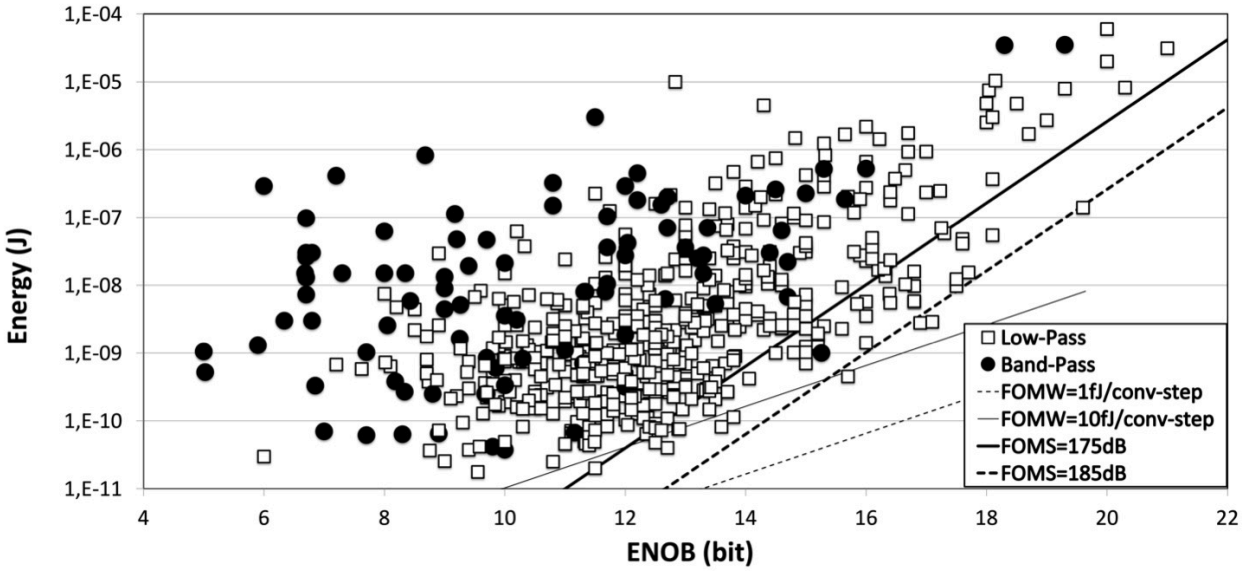

Figure 13. Energy plot of ΣΔMs: BP-ΣΔMs vs. LP-ΣΔMs.

As shown, the most efficient designs are based on LP-ΣΔMs—mostly implemented with CT circuits—some of them featuring a FOMS between 175 dB and 185 dB [100–108].

It is clear from Figure 13 that LP-ΣΔMs obtain better performance in terms of conversion energy than BP-ΣΔMs. However, it should be noted that the way in which such a conversion energy is computed—based on B_w—might not be adequate for quantifying the efficiency of BP-ΣΔMs because B_w is not always representative of the operating frequency of the modulator in this case. For that reason, some authors propose alternative FOMs, such as the following one [109]:

$$\text{FOM}_{\text{BP}}|_{\text{pJ/conv}} \equiv \frac{P_w(\text{W})}{2^{\text{ENOB(bit)}} \cdot (f_n + \frac{B_w}{2})} \cdot 10^{12} \tag{24}$$

which takes into account not only B_w but also the notch frequency, f_n to measure the conversion energy (E). The reader can note that the use of FOM_{BP} would increase the number of BP-ΣΔMs placed at the cutting edge of the state of the art, although the comparison

might be not so fair in this case for LP-ΣΔMs. This is illustrated in Figure 14, which shows the conversion energy redefined as

$$E_{\mathrm{BP}} \equiv \frac{P}{f_n + \frac{B_w}{2}} \tag{25}$$

As will be discussed later, new generations of BP-ΣΔMs are being developed in order to make RF digitizers more feasible. Thus, it is interesting to compare the performance of BP-ΣΔMs in terms of different architectures, circuits and systems techniques. According to the discussion above, especial emphasis will be put not only on B_w but also on f_n.

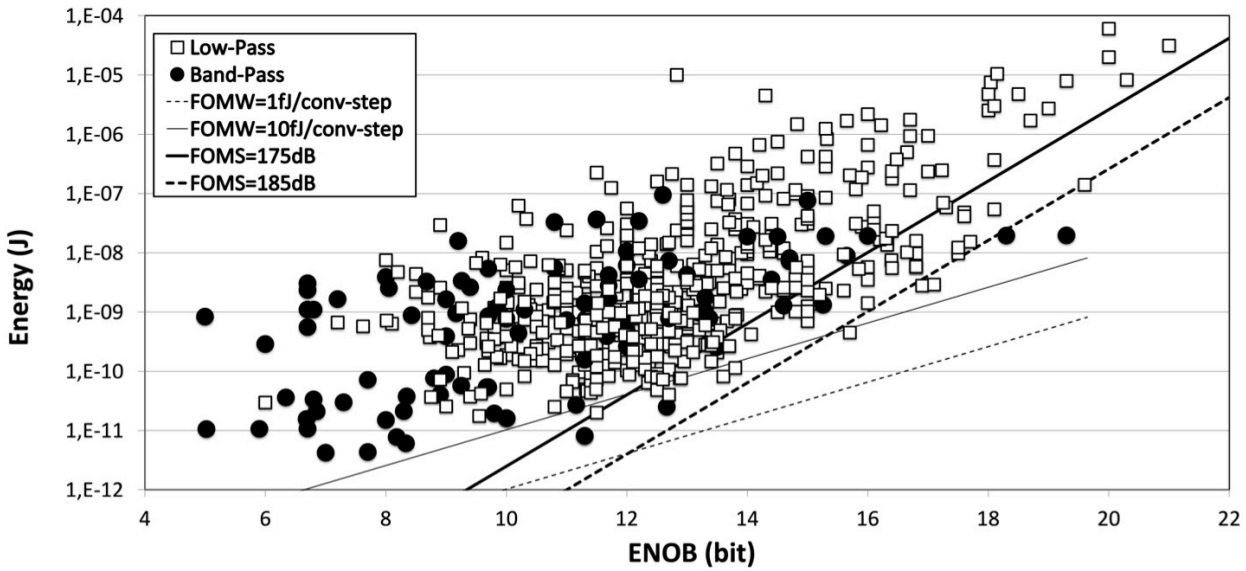

Figure 14. Energy plot of ΣΔMs using Equation (25) to compute the conversion energy of BP-ΣΔMs.

4.2. Comparison of Different Architectures and Circuits of BP-ΣΔMs

Figure 15a compares the performance of SC and CT BP-ΣΔMs by plotting ENOB vs. f_n. As one may expect, the notch frequencies of CT BP-ΣΔMs are higher than their SC counterparts. The f_n of SC implementations ranges from 1 MHz to less than 50 MHz, whereas CT BP-ΣΔMs digitize signals placed at carrier frequencies ranging from 100 kHz to 3 GHz [34]. The same happens if the digitized bandwidth, B_w, is considered as depicted in Figure 15b. In this case, CT BP-ΣΔMs also covers a wider range of B_w, ranging from 3 kHz to almost 300 MHz [88], with 19.3-bit to 8.3-bit ENOB, respectively. More details about the performance metrics achieved by SC and CT BP-ΣΔMs are shown in Tables 1 and 2, respectively. Under similar requirements, the energy consumed by CT BP-ΣΔMs is less than that obtained by SC BP-ΣΔMs as illustrated in the energy plot shown in Figure 15c.

Figure 16 compares CT BP-ΣΔMs in terms of the circuit techniques used to implement the loop filter (LF), namely, LC-based or *inductorless*, i.e., Gm-C, and active-RC. Although the highest notch frequencies are reached by LC-based BP-ΣΔMs, there is not a clear advantage with respect to inductorless implementations as depicted in Figure 16a. In terms of energy, inductorless implementations are more efficient as illustrated in Figure 16b, reaching higher resolutions (over 12-bit ENOB). Contrary to what might be expected, LC-based BP-ΣΔMs are not necessarily better to digitize RF signals when compared to BP-ΣΔMs based on active-RC/Gm-C resonators.

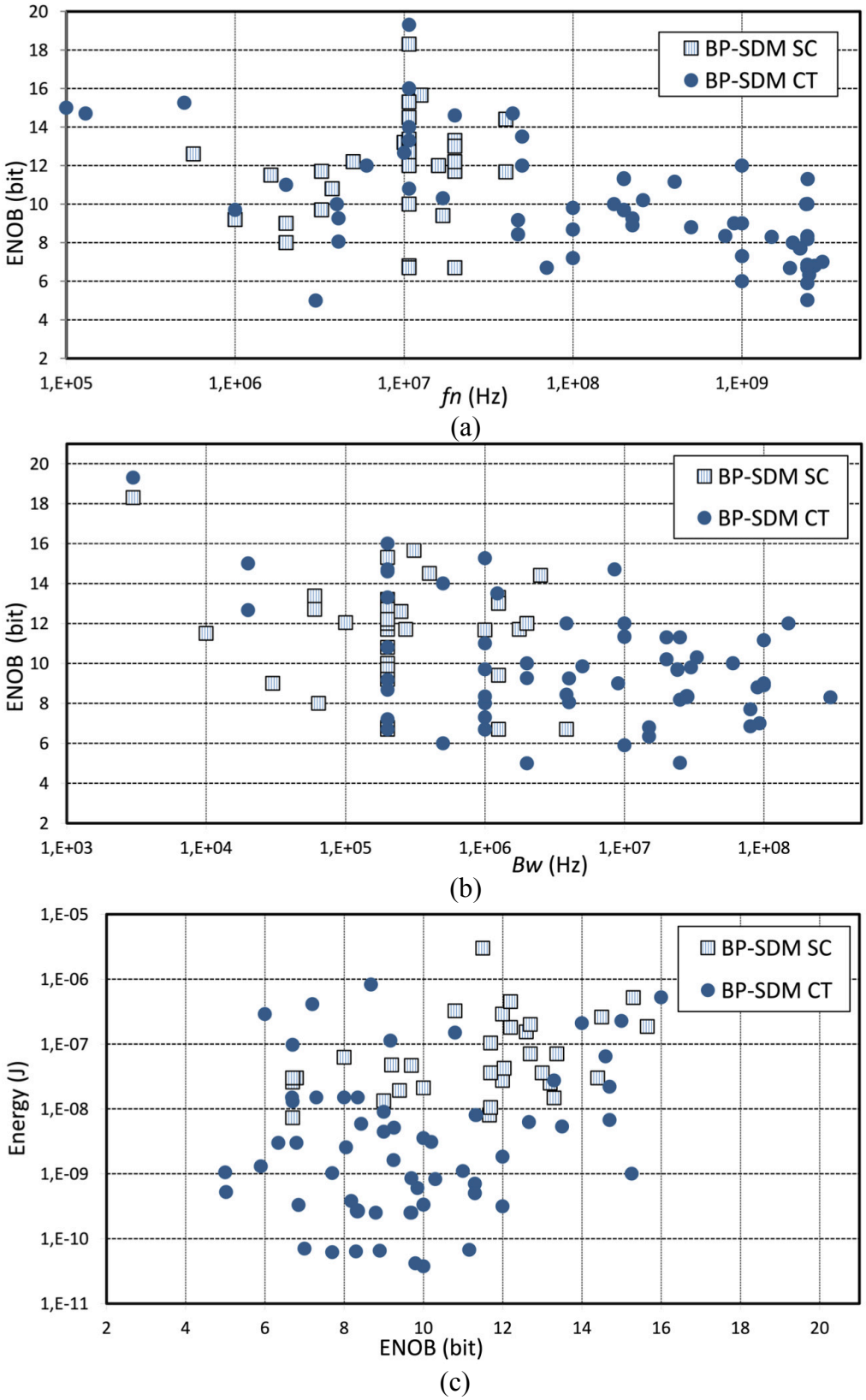

Figure 15. SC vs. CT BP-ΣΔMs: (**a**) ENOB vs. f_n, (**b**) ENOB vs. B_w. (**c**) Energy plot.

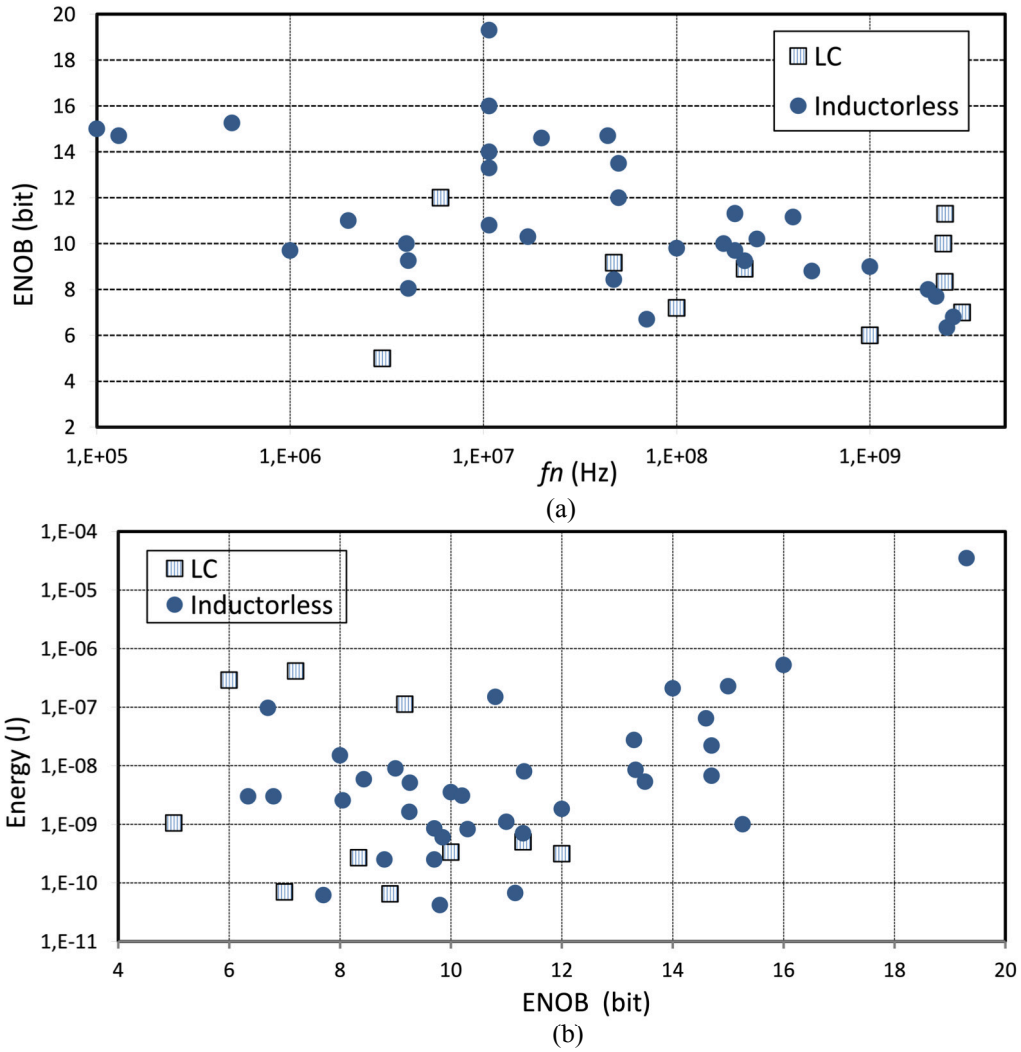

Figure 16. LC-based vs. inductorless BP-ΣΔMs: (**a**) ENOB vs. f_n, (**b**) energy plot.

Figure 17 shows the performance of CT BP-ΣΔMs in terms of the loop-filter order, L, by comparing those architectures with a 2nd-order ($L = 2$) loop filter and those with $L > 2$. There is not a clear benefit in terms of frequency operation by increasing the order, as shown in Figure 17a, although the ENOB improves with L, as expected. However, if the target ENOB is less than 12-bit, 2nd-order loop filters are more energy efficient than high-order architectures as illustrated in Figure 17b.

Figure 18 compares single-bit vs. multi-bit CT BP-ΣΔMs. The vast majority of BP-ΣΔMs uses a single-bit quantizer and dominates the state of the art, both in terms of frequency range, Figure 18a, and energy efficiency, Figure 18b. Multi-bit implementations are only advantageous if ENOB $<$ 12 bit, although there are more single-bit BP-ΣΔMs featuring higher resolutions in a wider tuning frequency range. This result is somehow logical since multi-bit quantization involves more complex dynamics in the loop filter, especially in the fast loop of CT BP-ΣΔMs. This is especially limiting when GHz-range clock signals are required.

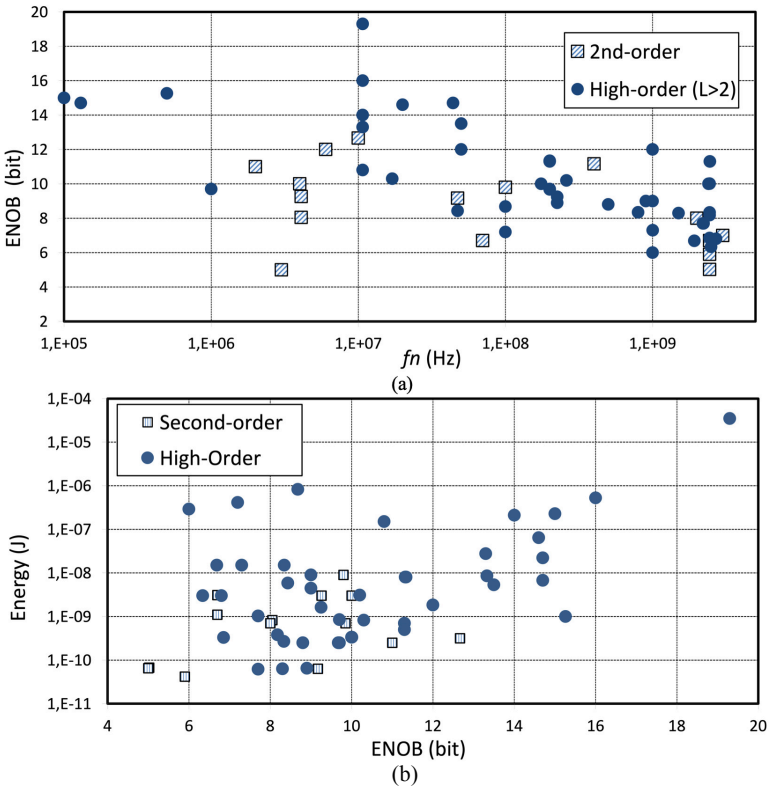

Figure 17. Second-order vs. High-order ($L > 2$) BP-ΣΔMs: (**a**) ENOB vs. f_n, (**b**) energy plot.

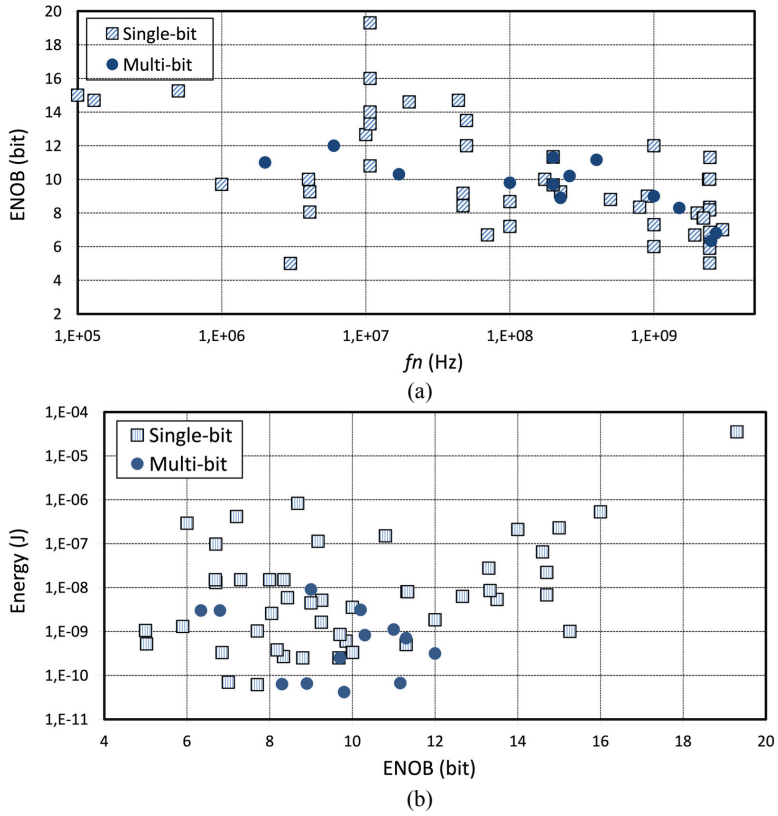

Figure 18. Single-bit vs. multi-bit BP-ΣΔMs: (**a**) ENOB vs. f_n, (**b**) energy plot.

4.3. Lessons Learned from State-of-the-Art BP-ΣΔMs

From the analysis of the state of the art described above, it can be concluded that low-order ($L = 2, 4$), single-bit CT BP-ΣΔMs are the best architectures in terms of operating frequency (f_n), ENOB and conversion energy. However, regardless of the architecture and circuit technique used, BP-ΣΔMs are not competitive yet with their LP counterparts, which explains why direct-conversion receivers are the preferred choice in mobile terminals even though they are sensitive to analog impairments of I/Q downconversion. In order to make BP-ΣΔMs more efficient for RF ADCs in SDR, it is needed to adopt circuit techniques which can increase the carrier (notch) frequency programmability, with reduced power consumption and (analog) hardware complexity.

Where the loop filter (LF) is concerned, highly programmable scaling-friendly amplifier stages, such as those based on inverter-based OTAs—originally proposed by Nauta [110]—are good candidates to implement both LC-based and active-(GmC) resonators. These circuits have been mostly used in LP-ΣΔMs, but very little has been done in BP-ΣΔMs [54]. Hybrid active/passive circuits, such as those used by Chae et al. [49], can be exploited to reduce the power dissipation of GHz-range BP-ΣΔMs. Moreover, switchable passive RC networks are also suited to implement reconfigurable LFs as well as frequency interleaving [88] and N-path structures. The latter has been used in BP-ΣΔMs, although limited to carrier frequencies in the range of hundreds of MHz [87]. However, N-path filters have demonstrated a widely tuning range in GHz filters [111]. This feature should be exploited in BP-ΣΔM RF ADCs.

Regarding the quantizer, a 1-bit ADC, i.e., a simple (regenerative latch) comparator, is the preferred choice by most state-of-the-art BP-ΣΔMs. Multi-bit quantization increases hardware complexity and dynamic requirements in GHz-clocked BP-ΣΔMs, as well as the linearity specifications of the feedback DAC. However, single-bit CT BP-ΣΔMs are more sensitive to clock jitter, which becomes one of the main limiting factors in RF ADCs. This problem can be palliated by using a finite-impulse response (FIR) feedback DAC since it filters the FS comparator output such that a two-level data sequence is transformed into multi-level data. This reduces the height of steps in the DAC waveform, thus reducing the magnitude of the error signal exciting the LF of the BP-ΣΔM. FIR-DACs have been widely used in CT LP-ΣΔMs, but their benefits have not been exploited yet in BP-ΣΔMs.

5. Conclusions

An early digitization is desired in multi-mode/multi-standard wireless transceivers and SDR systems. This approach allows to move most of the signal processing from the analog to the digital domain, thus benefiting from technology downscaling and a higher programmability. BP-ΣΔMs are a priori the best candidates to implement RF ADCs in SDRs since they directly digitize RF signals without the need for downmixing them to the baseband. In spite of these benefits, BP-ΣΔMs are less efficient than LP-ΣΔMs due to the demanding specifications required for the loop-filter circuit to operate at GHz carrier or notch frequencies. The lessons learned from the analysis of the state of the art on BP-ΣΔMs carried out in this paper yield the following conclusions:

- System-level: A more simple BP-ΣΔM architecture—based on a 2nd- or 4th-order loop filter and a 1-bit quantizer—achieves cutting-edge performance, being a good choice that balances performance and efficiency.
- Circuit-level: There are some circuit strategies which can improve the performance of BP-ΣΔMs in terms of power consumption, scaling and reconfigurability. Among others, the following techniques are good candidates: inverter-based OTAs, N-path filtering, FIR-filtered feedback DAC and embedded time/frequency-interleaving topologies.

The combination of the above circuits and systems strategies can enhance the efficiency of BP-ΣΔMs to digitize RF signals with the specifications required for SDR transceivers: 8-to-12 bit effective resolution within a programmable 30 kHz-to-300 MHz bandwidth and a tunable carrier frequency ranging from 0.4 GHz to 6 GHz.

Thirty years after the first BP-ΣΔM chip was published, the path toward an efficient RF ADC might be closer to making SDR-based mobile handsets a reality.

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